X20CP1301, X20CP1381 and X20CP1382

1 General information

Compact CPUs are available with processor speeds of 200 MHz and 400 MHz. Depending on the variant, up to 256 MB RAM and up to 32 kB nonvolatile onboard RAM is available. A built-in flash drive is available to store up to 2 GB of application and other data.

All CPUs come equipped with Ethernet, USB and one RS232 interface. In both performance classes, integrated POWERLINK and CAN bus interfaces are also available. If additional fieldbus connections are needed, all CPUs can be upgraded with an interface module from the standard X20 product range. These CPUs do not require fans or batteries and are therefore maintenance-free. 30 different digital inputs and outputs and two analog inputs are integrated in the devices. One analog input can be used for PT1000 resistance temperature measurement.

- CPU is Intel® ATOM™ 400 MHz compatible with integrated I/O processor
- Ethernet, POWERLINK with poll-response chaining and USB onboard
- 1 slot for modular interface expansion
- 30 digital inputs/outputs and two analog inputs integrated in the device
- 1/2 GB flash drive onboard
- 128/256 MB DDR3 SDRAM
- Fanless
- No battery
- Battery-backed real-time clock

2 Order data

Model number	Short description
	X20 CPUs
X20CP1301	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 1 GB flash drive onboard, 1 insert slot for X20 interface modules, 1 USB interface, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including power supply module, 3x X20TB1F terminal blocks, slot cover and X20 locking plate X20AC0SR1 (right) included
X20CP1381	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included
X20CP1382	X20 CPU, with integrated I/O, x86-400, 256 MB DDR3 RAM, 32 kB FRAM, 2 GB flash drive on board, 2 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included

Table 1: Order data

Content of delivery

Model number	Quantity	Short description
-	1	Interface module slot cover
X20AC0SR1	1	X20 locking plate, right
X20TB1F	3	X20 terminal block, 16-pin, 24 VDC keyed

Table 2: Content of delivery

3 Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
Short description			
Interfaces	1x RS232, 1x Ethernet, 1x USB, 1x X2X Link	1x RS232, 1x Ethernet, 1x POWERLINK, 2x USB, 1x X2X Link, 1x CAN bus	
System module	CPU		
General information			
Cooling	Fanless		
B&R ID code	0xE35B	0xE35C	0xDABB
Status indicators	CPU function, Ethernet, RS232, CPU supply, I/O supply, I/O function per channel	CPU function, Ethernet, POWERLINK, RS232, CAN bus, CAN bus terminating resistor, CPU supply, I/O supply, I/O function per channel	
Diagnostics			
Outputs	Digital outputs: Yes, using status LED and software (output error status)		
CPU function	Yes, using status LED		
CAN bus data transfer	-	Yes, using status LED	
RS232 data transfer	Yes, using status LED		
Inputs	Analog inputs: Yes, using status LED and software		
Ethernet	Yes, using status LED		
I/O supply	Yes, using status LED		
POWERLINK	-	Yes, using status LED	
Supply voltage monitoring	Yes, using status LED		
Overtemperature	Yes, using software		
Terminating resistors	-	Yes, using status LED	
CPU redundancy possible	No		
ACOPOS capability	Yes		
reACTION-capable I/O channels	No		
Visual Components support	Yes		
Power consumption without interface module and USB	TBD		
Internal power consumption of the X2X Link and I/O supply [1)]			
Bus	TBD		
Internal I/O	TBD		
Additional power dissipation caused by the actuators (resistive) [W]	-		
Electrical isolation			
Power supply			
I/O feed - I/O supply	No		
CPU/X2X Link feed - CPU/IF6	Yes		
IF1 - IF2	Yes		
IF1 - IF3	-	Yes	
IF1 - IF4	No		
IF1 - IF5	-	No	
IF1 - IF6	Yes		
IF1 - IF7	-	No	
IF2 - IF3	-	Yes	
IF2 - IF4	Yes		
IF2 - IF5	-	Yes	
IF2 - IF6	Yes		
IF2 - IF7	-	Yes	
IF3 - IF4	-	Yes	
IF3 - IF5	-	Yes	
IF3 - IF6	-	Yes	
IF3 - IF7	-	Yes	
IF4 - IF5	-	No	
IF4 - IF6	Yes		
IF4 - IF7	-	No	
IF5 - IF6	-	Yes	
IF5 - IF7	-	No	
IF6 - IF7	-	Yes	
Channel - Bus	Yes		
Channel - Channel	No		
Channel - PLC	No		
PLC - IF1 (RS232)	No		
PLC - IF2 (Ethernet)	Yes		
PLC - IF3 (POWERLINK)	-	Yes	
PLC - IF4 (USB)	No		
PLC - IF5 (USB)	-	No	
PLC - IF6 (X2X Link)	Yes		
PLC - IF7 (CAN bus)	-	No	
Certification			
CE	Yes		
GOST-R	Yes		

Table 3: Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
CPU and X2X Link supply			
Input voltage	24 VDC -15% / +20%		
Input current	Max. TBD A		
Fuse	Integrated, cannot be replaced		
Reverse polarity protection	Yes		
X2X Link supply output			
Nominal output power	2 W		
Parallel operation	Yes [2]		
Redundant operation	Yes [3]		
Input I/O supply			
Input voltage	24 VDC -15% / +20%		
Fuse	Required line fuse: Max. 10 A, slow-blow		
Output I/O supply			
Rated output voltage	24 VDC		
Permitted contact load	10 A		
Controller			
Real-time clock	Buffering for at least 300 hours at 25°C, 1 s resolution, -18 to 28 ppm accuracy at 25°C		
FPU	Yes		
Processor			
Type	Vx86EX		
Clock frequency	200 MHz		400 MHz
L1 cache			
Data code	16 kB		
Program code	16 kB		
L2 cache	128 kB		
Integrated I/O processor	Processes I/O data points in the background		
Modular interface slots	1		
Remanent variables	16 kB FRAM, buffering >10 years [4]		32 kB FRAM, buffering >10 years [4]
Shortest task class cycle time	2 ms		1 ms
Typical instruction cycle time	0.0419 µs		0.0199 µs
Standard memory			
RAM	128 MB DDR3 SDRAM		256 MB DDR3 SDRAM
Application memory			
Type	1 GB eMMC flash memory		2 GB eMMC flash memory
Data retention	10 years		
Writable data amount			
Guaranteed	40 TB		
Results for 5 years	21.9 GB/day		
Guaranteed clear/write cycles	20,000		
Error correction coding (ECC)	Yes		
Interfaces			
IF1 interface			
Signal	RS232		
Design	Connection made using 16-pin X20TB1F terminal block		
Max. distance	900 m		
Transfer rate	Max. 1152 kbit/s		
IF2 interface			
Signal	Ethernet		
Design	1x RJ45 shielded		
Cable length	Max. 100 m between 2 stations (segment length)		
Transfer rate	10/100 Mbit/s		
Transmission			
Physical interfaces	10BASE-T / 100BASE-TX		
Half-duplex	Yes		
Full-duplex	Yes		
Autonegotiation	Yes		
Auto-MDI / MDIX	Yes		
IF3 interface			
Fieldbus	-	POWERLINK managing or controlled node	
Type	-	Type 4 [5]	
Design	-	1x RJ45 shielded	
Cable length	-	Max. 100 m between 2 stations (segment length)	
Transfer rate	-	100 Mbit/s	
Transmission			
Physical interfaces	-	100BASE-TX	
Half-duplex	-	Yes	
Full-duplex	-	No	
Autonegotiation	-	Yes	
Auto-MDI / MDIX	-	Yes	
IF4 interface			
Type	USB 1.1/2.0		
Design	Type A		
Max. output current	0.5 A		

Table 3: Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
IF5 interface			
Type	-	USB 1.1/2.0	
Design	-	Type A	
Max. output current	-	0.1 A	
IF6 interface			
Fieldbus	X2X Link master		
IF7 interface			
Signal	-	CAN bus	
Design	-	Connection made using 16-pin X20TB1F terminal block	
Max. distance	-	1000 m	
Transfer rate	-	Max. 1 MBit/s	
Terminating resistors	-	Integrated in the module	
Controller	-	SJA 1000	
Digital inputs			
Quantity	14 standard inputs, 4 high-speed inputs and 4 mixed channels, configurable as inputs or outputs using software		
Nominal voltage	24 VDC		
Input voltage	24 VDC -15% / +20%		
Input current at 24 VDC	X1 - Standard inputs: Typ. 3.5 mA X2 - Standard inputs: Typ. 2.68 mA X2 - High-speed inputs: Typ. 3.5 mA X3 - Mixed channels: Typ. 2.68 mA		
Input filter			
Hardware	Standard inputs and mixed channels: ≤200 µs High-speed inputs: ≤2 µs, when used as standard inputs: ≤200 µs		
Software	Default 1 ms, configurable between 0 and 25 ms in 0.1 ms intervals		
Connection type	1-wire connections		
Input circuit	Sink		
Additional functions	X2 - High-speed digital inputs: 2x 250 kHz event counting, 2x AB counter, ABR incremental encoder, direction/frequency, period measurement, gate measurement, differential time measurement, edge counters, edge times		
Input resistance	X1 - Standard inputs: 6.8 kΩ X2 - Standard inputs: 8.9 kΩ X2 - High-speed inputs: 6.8 kΩ X3 - Mixed channels: 8.9 kΩ		
Switching threshold			
Low	<5 VDC		
High	>15 VDC		
AB incremental encoder			
Quantity	2		
Encoder inputs	24 V, asymmetrical		
Counter size	32-bit		
Input frequency	Max. 100 kHz		
Evaluation	4x		
Encoder supply	Module-internal, max. 300 mA		
Overload behavior of the encoder supply	Short circuit protection, overload protection		
ABR incremental encoder			
Quantity	1		
Encoder inputs	24 V, asymmetrical		
Counter size	32-bit		
Input frequency	Max. 100 kHz		
Evaluation	4x		
Encoder supply	Module-internal, max. 300 mA		
Overload behavior of the encoder supply	Short circuit protection, overload protection		
Event counter			
Quantity	2		
Signal form	Square wave pulse		
Evaluation	1x		
Input frequency	Max. 250 kHz		
Counter frequency	250 kHz		
Counter size	32-bit		
Time measurement			
Possible measurements	Period measurement, gate measurement, differential time measurement, edge counter, edge times		
Measurements per module	Each function up to 4x		
Counter size	32-bit		
Timestamp	1 µs resolution		
Signal form	Square wave pulse		
Analog inputs			
Quantity	2 [6)]		
Input	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections		
Input type	Differential input		
Digital converter resolution			
Voltage	±12-bit		
Current	12-bit		

Table 3: Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
Conversion time	1 channel enabled: 100 µs 2 channels enabled: 200 µs		
Output format			
Data type	INT		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV		
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA		
Input impedance in signal range			
Voltage	20 MΩ		
Current	-		
Load			
Voltage	-		
Current	<300 Ω		
Input protection	TBD: Protection against wiring with supply voltage		
Permitted input signal			
Voltage	Max. ±30 V		
Current	Max. ±50 mA		
Output of the digital value during overload	Configurable		
Conversion procedure	SAR		
Input filter	3rd-order low pass / cutoff frequency 1 kHz		
Max. error at 25°C			
Voltage			
Gain	0.18% (Rev. <C0: 0.37%) [7]		
Offset	0.04% (Rev. <C0: 0.25%) [8]		
Current			
Gain	0 to 20 mA = 0.15% (Rev. <C0: 0.52%) / 4 to 20 mA = 0.25% [7]		
Offset	0 to 20 mA = 0.1% (Rev. <C0: 0.4%) / 4 to 20 mA = 0.15% [9]		
Max. gain drift			
Voltage	0.017 %/°C [7]		
Current	0 to 20 mA = 0.015 %/°C / 4 to 20 mA = 0.023 %/°C [7]		
Max. offset drift			
Voltage	0.008 %/°C [8]		
Current	0 to 20 mA = 0.008 %/°C / 4 to 20 mA = 0.012 %/°C [9]		
Common-mode rejection			
DC	70 dB		
50 Hz	70 dB		
Common-mode range	±12 V		
Crosstalk between channels	<-70 dB		
Non-linearity			
Voltage	<0.025 % [8]		
Current	<0.05 % [9]		
Temperature inputs resistance measurement			
Quantity	1		
Input	Resistance measurement with constant current supply for 2-wire connections		
Digital converter resolution	13-bit		
Conversion time	Only temperature input enabled: 200 µs Temperature and analog input enabled: 400 µs		
Conversion procedure	SAR		
Output format	INT or UINT for resistance measurement		
Sensor			
PT1000	-200 to 850°C		
Resistance measurement range	01 to 4000 Ω		
Temperature sensor resolution	TBD: 1 LSB = 0.16°C		
Resistance measurement resolution	TBD: 1 LSB = 0.61 Ω		
Input filter	1st-order low pass / cutoff frequency 7 Hz		
Sensor standard	IEC/EN 60751		
Common-mode range	1 V		
Linearization method	Internal		
Measuring current	1 mA		
Permitted input signal	Short-term max. ±30 V		
Max. error at 25°C			
Gain	0.3% (Rev. <C0: 1.93%) [10]		
Offset	0.15% (Rev. <C0: 0.32%) [11]		
Max. gain drift	0.023 %/°C [10]		
Max. offset drift	0.012 %/°C [11]		
Non-linearity	<0.05 % [11]		
Standardized value range for resistance measurement	01 Ω to 40,000 Ω		
Crosstalk between channels	<-70 dB		
Common-mode rejection			
50 Hz	>60 dB		
DC	TBD		
Temperature sensor standardization			
PT1000	-200 to 850°C		

Table 3: Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
Digital outputs			
Design	Standard outputs and mixed channels: FET positive switching High-speed outputs: Push-Pull		
Quantity	4 standard outputs, 4 high-speed outputs and 4 mixed channels, configurable as inputs or outputs using software		
Nominal voltage	24 VDC		
Switching voltage	24 VDC -15% / +20%		
Nominal output current	Standard outputs and mixed channels: 0.5 A High-speed outputs: 0.2 A		
Total nominal current	Standard outputs and mixed channels: 4 A High-speed outputs: 0.8 A		
Connection type	1-wire connections		
Output circuit	Standard outputs and mixed channels: Source High-speed outputs: Sink or source		
Output protection [12]	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")		
Pulse width modulation [13]			
Period duration	5 to 65535 µs corresponds to 200 kHz to 15 Hz		
Pulse duration	0.0 to 100.0%, minimum 2.5 µs		
Resolution for pulse duration	0.1% of the configured frequency		
Diagnostic status	Standard outputs and mixed channels: Output monitoring with 10 ms delay High-speed outputs: Output monitoring with 10 µs delay		
Leakage current when switched off	Standard outputs and mixed channels: 5 µA High-speed outputs: 25 µA		
$R_{DS(on)}$	140 mΩ [14]		
Residual voltage	Standard outputs and mixed channels: <0.1 V at 0.5 A rated current High-speed outputs: <0.9 V at 0.1 A rated current		
Peak short circuit current	Standard outputs and mixed channels: <3 A High-speed outputs: <20 A		
Switching on after overload or short circuit cutoff	Standard outputs and mixed channels: Approx. 10 ms (depends on the module temperature) High-speed outputs: TBD		
Switching delay			
0 -> 1	Standard outputs and mixed channels: <300 µs High-speed outputs: <3 µs		
1 -> 0	Standard outputs and mixed channels: <300 µs High-speed outputs: <3 µs		
Switching frequency			
Resistive load [15]	Standard outputs and mixed channels: Max. 500 Hz High-speed outputs: 50 kHz, max. 200 kHz (see section "Switching frequency derating for high-speed digital outputs")		
Inductive load	See section "Switching inductive loads"		
Braking voltage when switching off inductive loads	Standard outputs and mixed channels: Typ. 45 VDC		
Operating conditions			
Mounting orientation			
Horizontal	Yes		
Vertical	Yes		
Installation at elevations above sea level			
0 to 2000 m	No limitations		
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m		
EN 60529 protection	IP20		
Environmental conditions			
Temperature			
Operation			
Horizontal installation	-25 to 60°C		-25 to 60°C (Rev. <D0: -25 to 55°C)
Vertical installation	TBD		
Derating	TBD		
Storage	-40 to 85°C		
Transport	-40 to 85°C		
Relative humidity			
Operation	5 to 95%, non-condensing		
Storage	5 to 95%, non-condensing		
Transport	5 to 95%, non-condensing		
Mechanical characteristics			
Note	X20 locking plate (right) included in delivery 3 X20 terminal blocks (16-pin) included in delivery Interface module slot cover included in delivery		
Dimensions			
Width	164 mm		
Height	99 mm		
Depth	75 mm		
Weight	300 g	310 g	

Table 3: Technical data

1) The values specified here are maximum values. The exact calculation is available with the other module documentation for download from the B&R website.
2) When operated in parallel, the nominal power of 2 W is not permitted to be added to the total power.
3) Up to 2 W bus load.
4) Can be set in Automation Studio.

5) See the POWERLINK section of the AS help system under "General information, Hardware - IF/LS".
6) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
7) Based on the current measured value.
8) Based on the 20 V measurement range.
9) Based on the 20 mA measurement range.
10) Based on the current resistance value.
11) Based on the entire resistance measurement range.
12) For high-speed digital outputs, derating must be applied at switching frequencies >50 kHz (see section "Switching frequency derating for high-speed digital outputs"). Overtemperature protection is not provided.
13) The high-speed digital outputs can be used for pulse width modulation.
14) Only for standard outputs and mixed channels.
15) Standard outputs and mixed channels: At loads ≤1 kΩ.

4 LED status indicators on the integrated X1 I/O slot

Figure	LED	Color	Status	Description
	E	Red	On	SERVICE mode
			Double flash	BOOT mode (during firmware update)[1]
	R	Green	On	Application running
		Red	On	Reset in progress
	RF	Yellow	On	SERVICE or BOOT mode
	SE	Green/Red		Status/Error LED. The statuses of this LED are described in section 4.1 ""S/E" LED".
	ET	Green	On	A link to the peer station has been established.
			Blinking	A link to the peer station has been established. Indicates Ethernet activity is taking place on the bus.
	PL	Green	On	A link to the POWERLINK peer station has been established.
			Blinking	A link to the POWERLINK peer station has been established. Indicates Ethernet activity is taking place on the bus.
	A1 - A2	Green	Off	Open line or disconnected sensor
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK
	1 - 4	Green		Input state of the corresponding digital input
	C	Yellow	On	CPU transmitting or receiving data via the CAN bus interface
	S	Yellow	On	CPU transmitting or receiving data via the RS232 interface
	T	Yellow	On	The terminating resistor integrated in the CPU is switched on.
	DC	Yellow	On	CPU power supply OK

Table 4: LED status indicators on the integrated X1 I/O slot

1) A firmware update can take several minutes depending on the configuration.

4.1 "S/E" LED

The Status/Error LED is a green/red dual LED. The LED status can have different meanings depending on the operating mode.

4.1.1 Ethernet mode

In this mode, the interface is operated as an Ethernet interface.

Green - Status	Description
On	Interface operated as an Ethernet interface

Table 5: Status/Error LED - Ethernet operating mode

4.1.2 POWERLINK

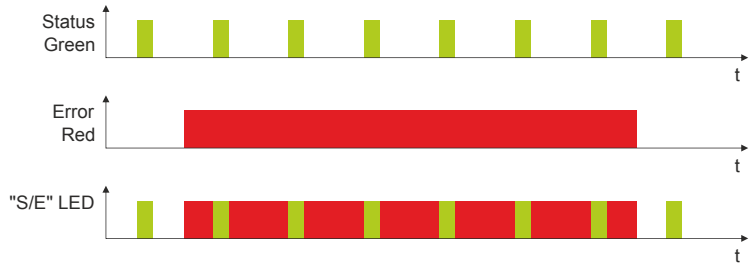
Red - Error	Description
On	The module is in an error mode (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: The LED blinks red several times immediately after startup. This is not an error.

Table 6: Status/Error LED as Error LED - POWERLINK operating mode

Green - Status	Description
Off	**Mode** The module is in NOT_ACTIVE mode or: • Switched off • Starting up • Not configured correctly in Automation Studio • Defective **Managing node (MN)** The bus is monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module will immediately enter PRE_OPERATIONAL_1 mode. If POWERLINK communication is detected before the time expires, however, then the MN will not be started. **Controlled node (CN)** The bus is monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module will immediately enter BASIC_ETHERNET mode. If POWERLINK communication is detected before this time passes, however, then the module will immediately go into PRE_OPERATIONAL_1 mode.
Green flickering (approx. 10 Hz)	**Mode** The module is in BASIC_ETHERNET mode. The interface is being operated as an Ethernet TCP/IP interface. **Managing node (MN)** This state can only be changed by resetting the module. **Controlled node (CN)** If POWERLINK communication is detected while in this state, the module will transition to the PRE_OPERATIONAL_1 state.
Single flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_1 mode. **Managing node (MN)** The MN starts "reduced cycle" operation. Cyclic communication is not yet taking place. **Controlled node (CN)** The module can be configured by the MN in this state. The CN waits until it receives an SoC frame and then transitions to the PRE_OPERATIONAL_2 state. An LED lit red in this state indicates a failure of the MN.
Double flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_2 mode. **Managing node (MN)** The MN begins cyclic communication (cyclic input data is not yet evaluated). The CNs are configured in this state. **Controlled node (CN)** The module can be configured by the MN in this state. A command then changes the state to READY_TO_OPERATE. An LED lit red in this mode indicates a failure of the MN.
Triple flash (approx. 1 Hz)	**Mode** The module is in the READY_TO_OPERATE state. **Managing node (MN)** Cyclic and asynchronous communication. The received PDO data is ignored. **Controlled node (CN)** The module configuration is complete. Normal cyclic and asynchronous communication. The PDO data sent corresponds to the PDO mapping. Cyclic data is not yet evaluated, however. An LED lit red in this mode indicates a failure of the MN.
On	**Mode** The module is in PRE_OPERATIONAL_2 mode. PDO mapping is active and cyclic data is being evaluated.
Blinking (approx. 2.5 Hz)	**Mode** The module is in STOPPED mode. **Managing node (MN)** This status is not possible for the MN. **Controlled node (CN)** No output data is produced or input data supplied. It is only possible to enter or leave this mode after the MN has given the appropriate command.

Table 7: Status/Error LED as Status LED - POWERLINK operating mode

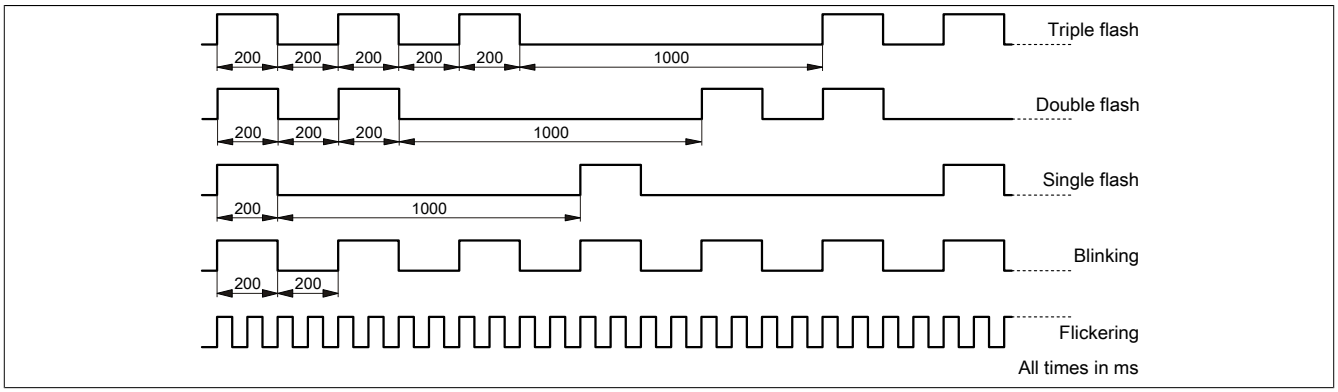


Figure 1: LED status indicators - Blinking patterns

4.2 System failure error codes

Incorrect configuration or defective hardware can cause a system failure error code.

The error code is indicated by the red Error LED using four switch-on phases. The switch-on phases have a duration of either 150 ms or 600 ms. The error code is output cyclically every 2 seconds.

Error description	Error code indicated by red status LED									
RAM error: The module is defective and must be replaced.	•	•	•	-	Pause	•	•	•	-	Pause
Hardware error: The module or a system component is defective and must be replaced.	-	•	•	-	Pause	-	•	•	-	Pause

Table 8: Status/Error ("S/E") LED - System failure error codes

Key: • ... 150 ms
- ... 600 ms
Pause ... 2 second delay

5 LED status indicators on the integrated X2 I/O slot

Figure	LED	Color	Status	Description
	1 - 14	Green		Input state of the corresponding digital input

Table 9: LED status indicators on the integrated X2 I/O slot

6 LED status indicators on the integrated X3 I/O slot

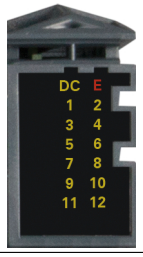
Figure	LED	Color	Status	Description
	DC	Yellow	On	I/O supply OK
	E	Red	Off	Everything OK
			Double flash	No power to module
	1 - 4	Yellow		Output status of the corresponding digital output
	5 - 8	Yellow		Input or output status of the corresponding digital input or output
	9 - 12	Yellow		Output status of the corresponding high-speed digital output

Table 10: LED status indicators on the integrated X3 I/O slot

7 Operating and connection elements

X20CP1301

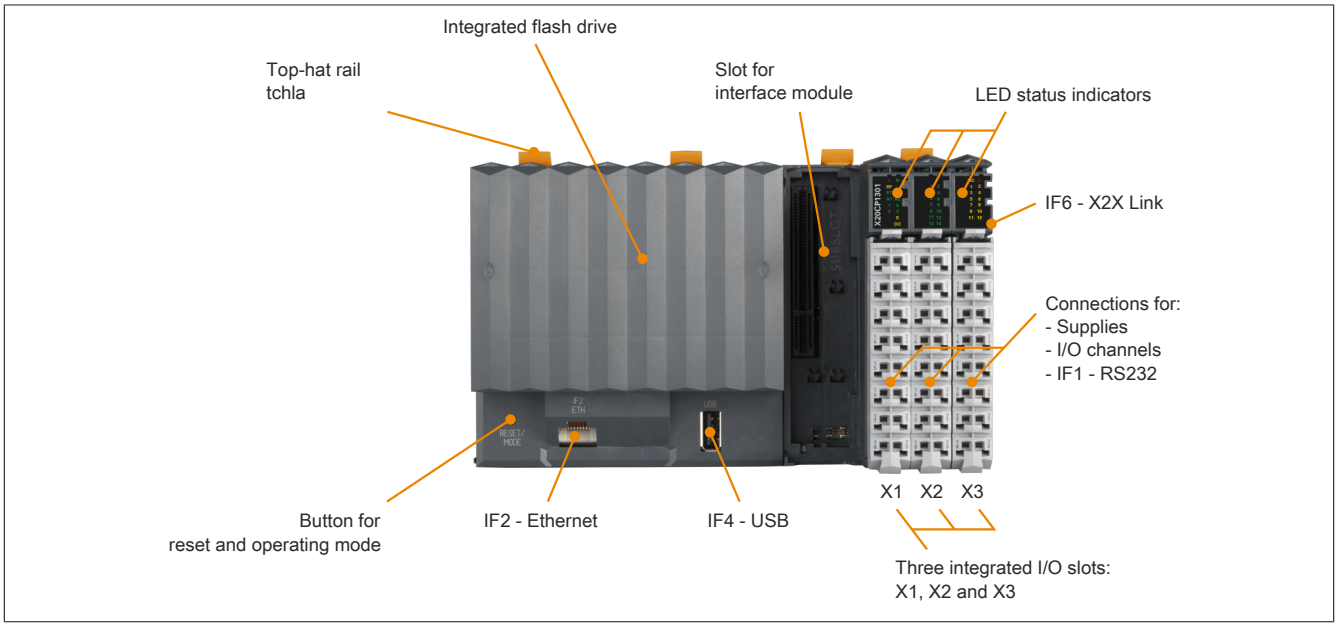


Figure 2: Operating elements for X20CP1301

X20CP1381 and X20CP1382

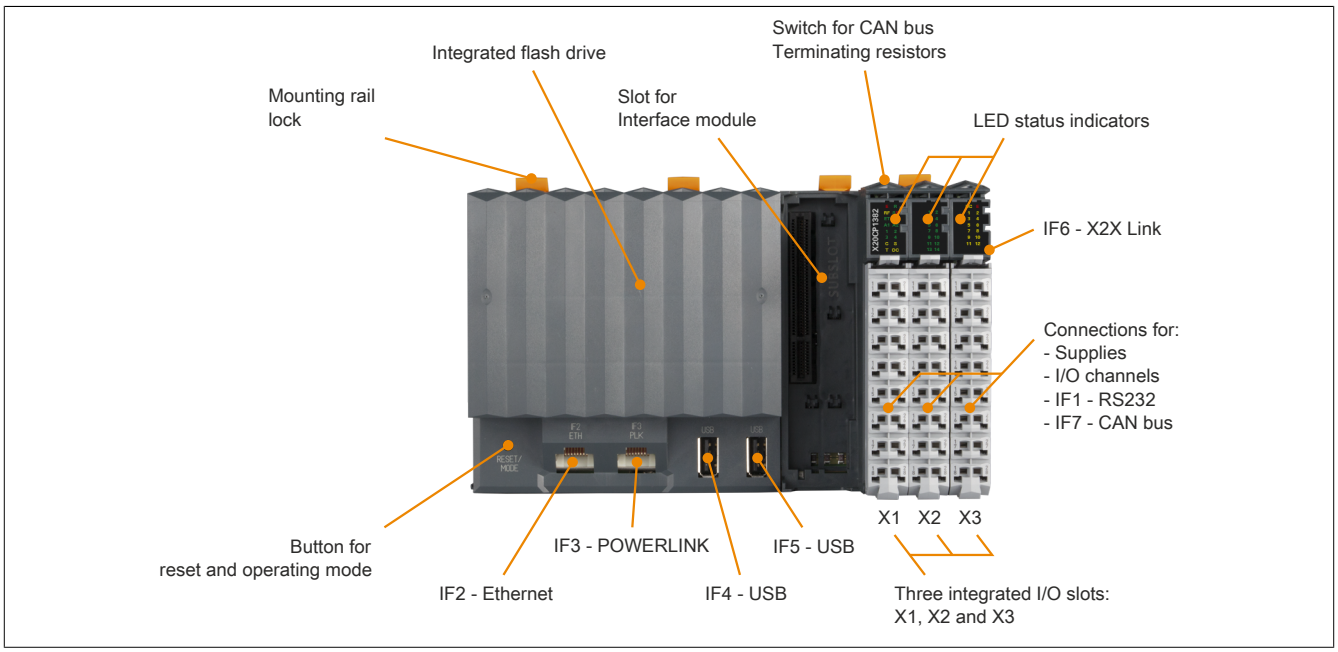


Figure 3: Operating elements for X20CP1381 and X20CP1382

8 Flash drive

These CPUs require application memory in order to operate. This application memory is integrated on a flash drive.

9 Reset and operating mode button

Figure 4: Reset and operating mode button

9.1 Reset

The button must be pressed for less than 2 seconds to trigger a reset. This triggers a hardware reset on the CPU, which means that:

- All application programs are stopped.
- All outputs are set to zero.

The PLC then boots into service mode by default. The boot mode that follows after pressing the reset button can be defined in Automation Studio.

- Service mode (default)
- Warm restart
- Cold restart
- Diagnostic mode

9.2 Operating mode

Three operating modes can be configured using different button sequences:

Operating mode	Button sequence	Description
BOOT	Boot mode is enabled by the following button sequence: • Press the button for less than two seconds. As soon as the "R" LED on the X1 I/O slot is lit **RED**, the button can be released. • Then press the button within two seconds for longer than two seconds. As soon as the "R" LED is no longer lit, the button can be released.	The default Automation Runtime system is started and the runtime system can be installed via the online interface (Automation Studio). User flash memory is deleted only after the download begins.
RUN	Press the button for less than two seconds. As soon as the "R" LED on the X1 I/O slot is lit **RED**, the button can be released.	RUN mode: The triggering and boot behavior are the same as what happens when a hardware reset is triggered (see section 9.1 "Reset" on page 13).
DIAGNOSE	Press the button for more than 2 seconds. The "R" LED on the X1 I/O slot lights up **RED** and then goes out. As soon as the "R" LED is no longer lit, the button can be released.	Boots the CPU in diagnostic mode. Program sections in User RAM and User FlashPROM are not initialized. After diagnostic mode, the CPU always boots with a cold restart.

Table 11: Operating mode description

10 CPU supply

A power supply is integrated in these compact CPUs. It has a feed for the CPU, X2X Link and the internal I/O supply. The supply for the CPU and X2X Link is electrically isolated.

The connections are located on the X3 I/O slot.

10.1 Compact CPU supply concept

To ensure proper operation of compact CPUs, the following items must be taken into consideration:

The supply concept	Description
CPU and I/O GND	The GND contact is provided five times on the terminal blocks of the integrated I/O slots. All GND contacts are connected to one another. The GND contacts of the CPU and I/O supply therefore use the same voltage.
Plug-in X20 I/O modules	Supply of X20 I/O modules that can be connected to the compact CPU: • X2X Link: Supplied by the CPU supply • I/O channels: Supplied by the I/O supply
Integrated X1 I/O slot	All digital and analog signals as well as the RS232 and CAN bus interface are supplied by the CPU supply. Their operation is therefore guaranteed even if there is no I/O supply.
Integrated X2 I/O slot	• All digital signals are supplied by the CPU supply. Their operation is therefore guaranteed even if there is no I/O supply. • The encoder supply is supplied by the I/O supply. If the encoder is not to be connected to the E-stop chain, then it must be connected to an external power supply or it will be supplied by the CPU supply.
Integrated X3 I/O slot	• All 12 digital signals are supplied by the I/O supply. • The status messages for each channel also work without an I/O supply. This guarantees that status messages will continue to be transferred during an E-stop. • The status of the I/O supply is indicated by a separate status message. **Caution!** **Channels 5 to 8 are designed as mixed channels. If one of these channels is being used, it is absolutely essential to ensure that there is no external voltage present on the I/O channel when the I/O supply is cut off. Otherwise, power will be regenerated back to the plus terminal of the I/O supply via the I/O channel. This will result in defective components.** **The following solutions are available for preventing power regeneration from occurring:** • **The I/O supply of the CPU is not permitted to be switched off, which allows the reference potential to be maintained.** • **If the I/O supply is switched off anyway (e.g. as part of the E-stop chain), then the sensor/actuator supplies must also be switched off. This prevents potential power regeneration and protects components from being destroyed.**

Table 12: Compact CPU supply concept

10.2 Pinout

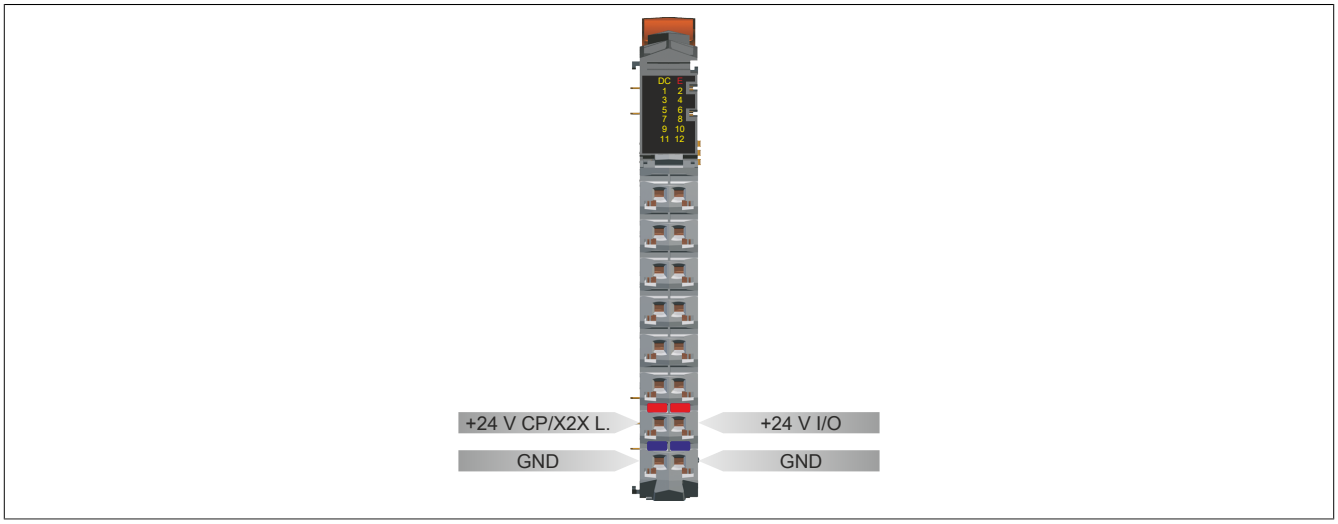


Figure 5: Integrated power supply - Pinout

10.3 Connection example

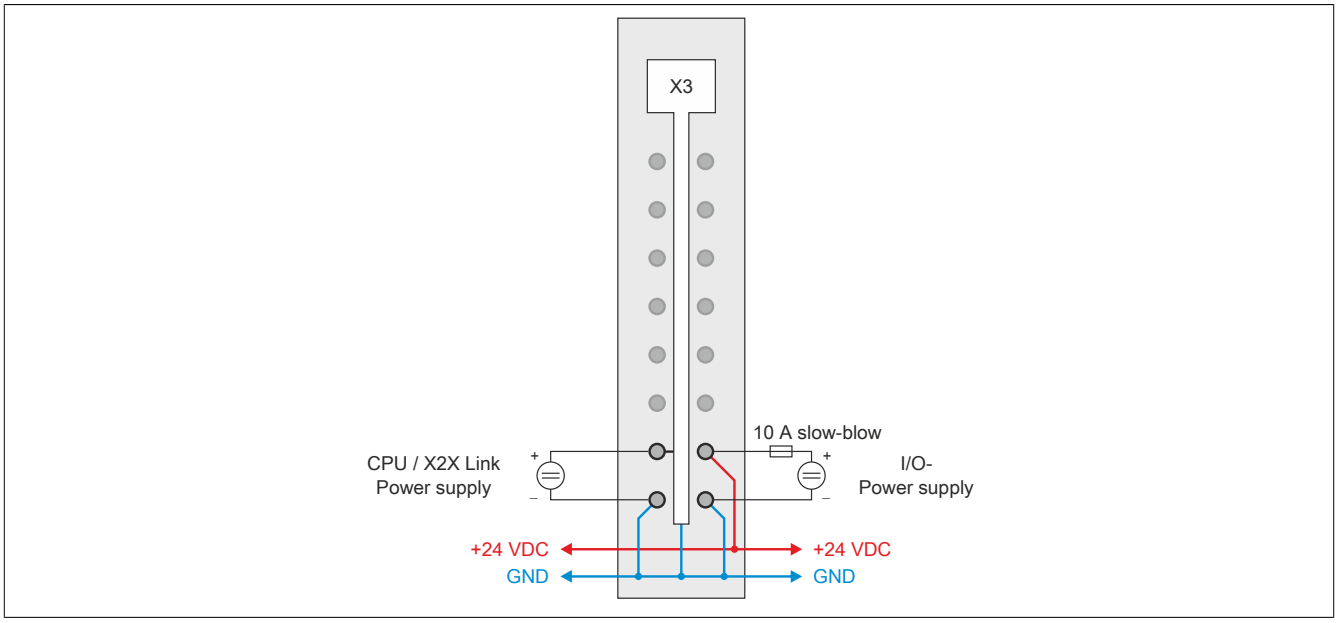


Figure 6: CPU supply - Connection example

11 RS232 interface (IF1)

The non-electrically isolated RS232 interface is primarily intended to serve as an online interface for communication with the programming device. It is located on the X1 I/O slot.

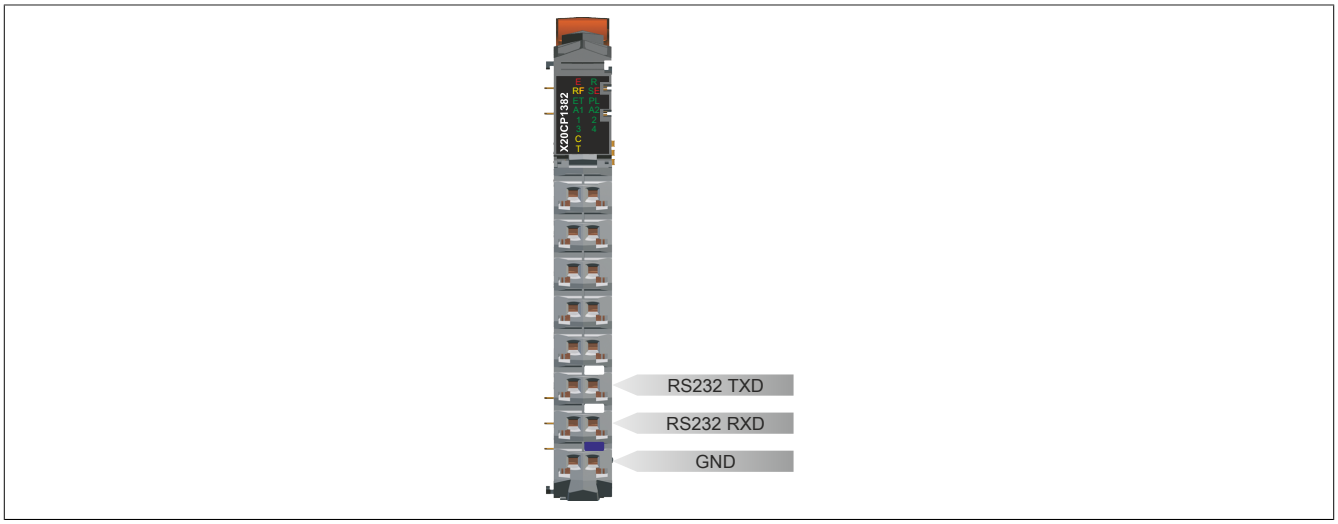
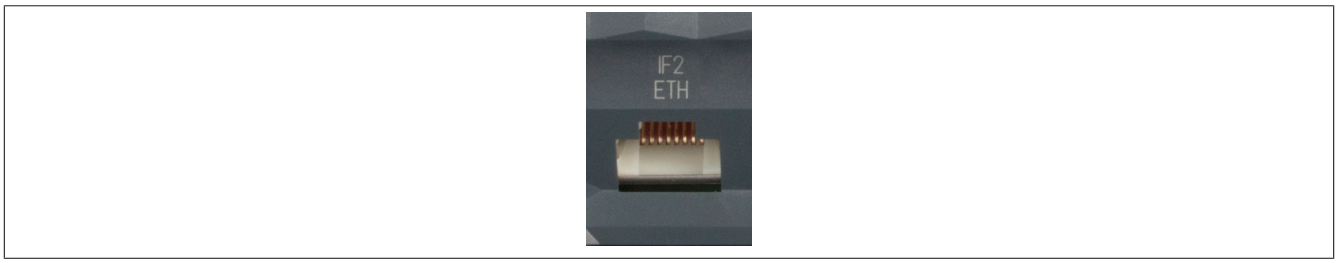


Figure 7: RS232 interface (IF1) on the X1 I/O slot - Pinout

12 Ethernet interface (IF2)



The IF2 interface is designed for 10BASE-T / 100BASE-TX transmission.

The INA2000 station number can be set using the Automation Studio software.

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section at www.br-automation.com.

Information:

The Ethernet interface (IF2) is not suited for POWERLINK (see section 13 "POWERLINK interface (IF3)" on page 17).

Pinout

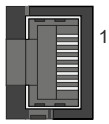
Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	TXD	Transmit data
	2	TXD\	Transmit data\
	3	RXD	Receive data
	4	Termination	
	5	Termination	
	6	RXD\	Receive data\
	7	Termination	
	8	Termination	

Table 13: Pinout

13 POWERLINK interface (IF3)

Compact CPUs X20CP1381 and X20CP1382 are equipped with a POWERLINK interface.

POWERLINK

Node numbers between 0x01 and 0xF0 are permitted. The node number can be configured using software.

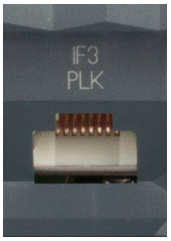
Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node. Operation as a controlled node.
0xF0	Operation as a managing node.
0xF1 - 0xFF	Reserved, switch position not permitted

Table 14: POWERLINK node number

Ethernet mode

In this mode, the interface is operated as an Ethernet interface. The INA2000 station number can be set using the Automation Studio software.

Pinout



Information about cabling X20 modules with an Ethernet interface can be found in the module's download section at www.br-automation.com.

Pin	Assignment	
1	RxD	Receive data
2	RxD\	Receive data\
3	TxD	Transmit data
4	Termination	
5	Termination	
6	TxD\	Transmit data\
7	Termination	
8	Termination	

Table 15: POWERLINK interface (IF3) - Pinout

14 USB interfaces (IF4 and IF5)

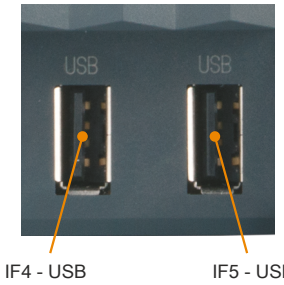


Figure 8: USB interfaces (IF4 and IF5)

IF4 and IF5 are non-electrically isolated USB interfaces. The connection is made using a USB 2.0 interface. Only IF4 is available on the entry level CPU.

The USB interfaces can only be used for devices approved by B&R (e.g. floppy disk drive, DiskOnKey or dongle).

Information:

- **USB interfaces cannot be used for online communication with a programming device.**
- **Only devices isolated from GND can be connected to the USB interfaces.**
- **The USB interfaces can handle up to the following current:**
  - **IF4: Max. 0.5 A**
  - **IF5: Max. 0.1 A**

15 CAN bus interface (IF7)

With the exception of the entry level CPU, all compact CPUs are equipped with a non-electrically isolated CAN bus interface. It is located on the X1 I/O slot.

15.1 Pinout

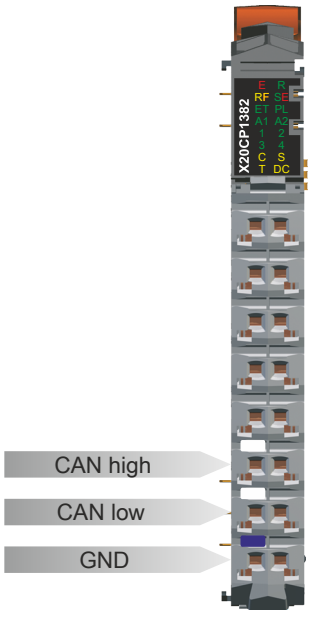


Figure 9: CAN bus interface (IF7) on the X1 I/O slot - Pinout

15.2 Terminating resistors

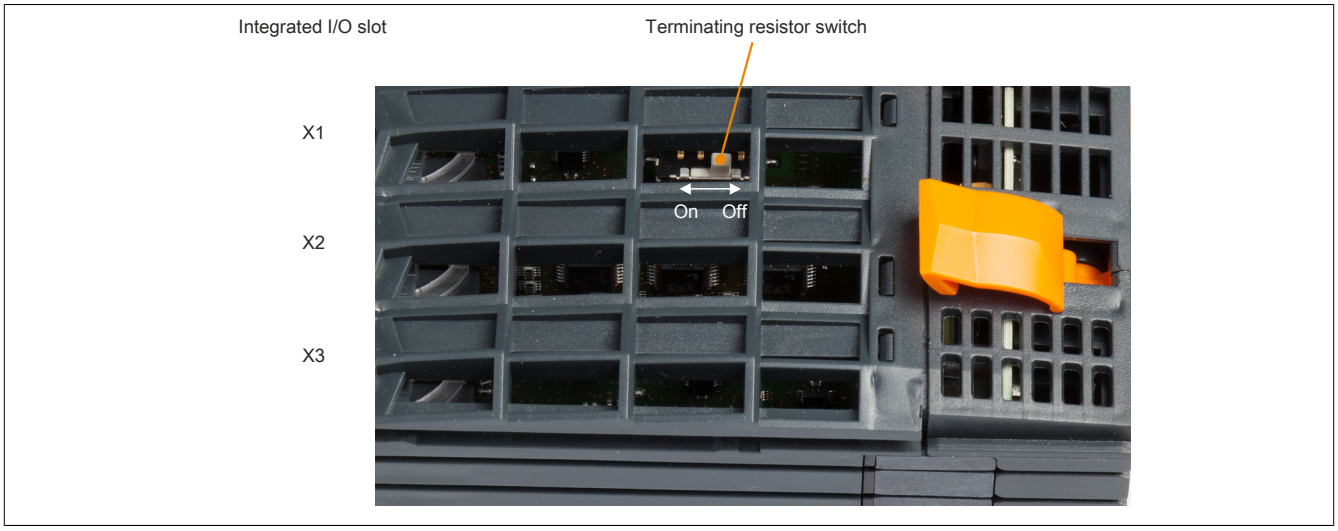


Figure 10: Switch positions for the CAN bus terminating resistor

A terminating resistor is already installed on the X1 I/O slot. It can be turned on and off with a switch on top of the housing. An active terminating resistor is indicated by the "T" LED.

16 Slot for interface modules

These CPUs are equipped with one slot for interface modules.

Various bus and network systems can easily be integrated into the X20 system by selecting the corresponding interface module.

17 Overtemperature cutoff

To prevent damage, a shutdown/reset is triggered on the CPU when the processor reaches 95°C.

The following errors are entered in the logbook:

Error number	Error description
9204	WARNING: System halted because of temperature check
9210	WARNING: Boot by watchdog or manual reset

Table 16: Logbook entries after overtemperature cutoff

18 Data and real-time clock buffering

Compact CPUs are not designed for use with batteries. This makes them completely maintenance-free. The following features make operation without a backup battery possible.

Data and real-time clock buffering	Type of buffering	Note
Remanent variables	FRAM	This FRAM stores its contents ferroelectrically. Unlike normal SRAM, this does not require a battery.
Real-time clock	Gold foil capacitor	The real-time clock is buffered for approx. 1000 hours by a gold foil capacitor. The gold foil capacitor is completely charged after 3 continuous hours of operation.

19 Programming the system flash memory

General information

In order for the application project to be executed on the CPU, the Automation Runtime operating system, system components and application project must be installed on the flash drive.

Installation over an online connection

These CPUs come standard with an Automation Runtime system (with limited functionality) already installed. This runtime system is started in boot mode (see section 9 "Reset and operating mode button" on page 13 or an invalid flash drive). Some of its tasks include initializing the Ethernet and integrated serial RS232 interfaces so that it is possible to download a runtime system.

1. Switch on the supply voltage for the CPU. The CPU starts with the default Automation Runtime in boot mode (see section 9 "Reset and operating mode button" on page 13 or an invalid flash drive).
2. Establish a physical online connection between the programming device (PC or industrial PC) and the CPU (e.g. over an Ethernet network or the RS232 interface).
3. Before you can establish an online connection via Ethernet, the CPU must be assigned an IP address. Search for available B&R target system in the local network by selecting **Online / Settings** from the Automation Studio menu and then clicking the **Browse targets** button. The CPU should appear in the list. If the CPU has not already received an IP address from a DHCP server, right-click on it and select **Set IP parameters** from the shortcut menu. All necessary network configurations can be made on a temporary basis in this dialog box (should be identical to the settings defined in the project).
4. Configure an online connection in Automation Studio. For details about the configuration: See AS help system under "Automation Software / Communication / Online communication"
5. Start the download procedure by selecting **Services** from the **Project** menu. Then select **Transfer Automation Runtime** from the pop-up menu. Now follow the instructions provided by Automation Studio.

20 I/O channels

Compact CPUs are equipped with three integrated I/O slots. These devices have 30 digital inputs/outputs and two analog inputs. One analog input can also be used for PT1000 resistance temperature measurement.

Information about the functions of the high-speed digital inputs and outputs can be found in the section 24 "Functions of the high-speed digital inputs/outputs" on page 26.

Overview of available I/O channels:

Integrated I/O	Quantity	I/O slot	Description
Digital inputs	14	X1: DI 1 to DI 4 X2: DI 1 to DI 10	24 VDC, sink, ≥0.5 ms, configurable software filter
High-speed digital inputs	4	X2: DI 11 to DI 14	24 VDC, sink, 2 µs, configurable software filter
Digital outputs	4	X3: DO 1 to DO 4	24 VDC, 0.5 A, source
Fast digital outputs	4	X3: DO 9 to DO 12	24 VDC, 0.2 A, 2 µs
Digital inputs/outputs	4	X3: DI 5 / DO 5 to DI 8 / DO 8	24 VDC, 0.5 A, configurable software filter
Analog inputs	2	X1: AI 1 to AI 2	±10 V / 0 to 20 mA or 4 to 20 mA, 12-bit, 1 ms
Temperature inputs	1	X1: AI 1 (Sensor + and Sense -)	PT1000 resistance temperature measurement Measurement takes place using the AI 1 analog input.

Table 17: I/O channels on compact CPUs

21 Pinout

X1 I/O slot - Pinout

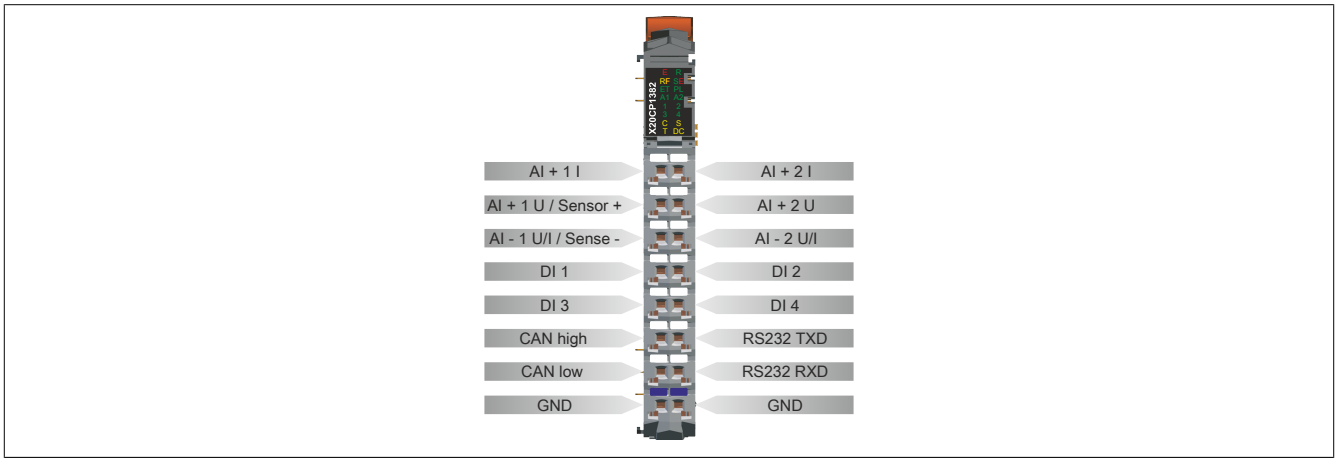


Figure 11: Pinout of the integrated X1 I/O slot

X2 I/O slot - Pinout

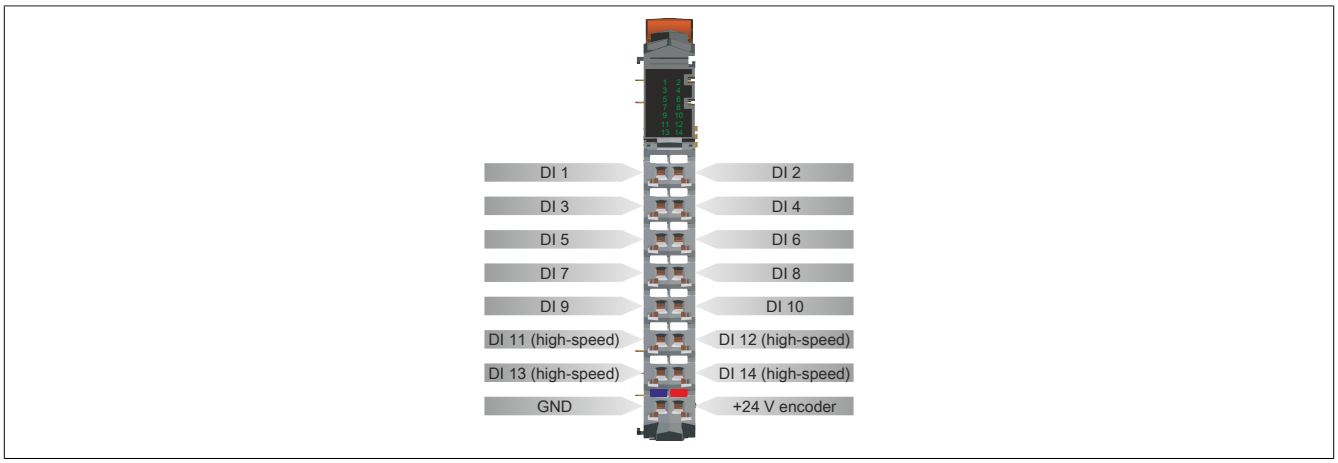


Figure 12: Pinout of the integrated X2 I/O slot

X3 I/O slot - Pinout

To ensure proper operation of the digital mixed channels (DI 5 / DO 5 to DI 8 / DO 8), it is important to observe the notes in section 10.1 "Compact CPU supply concept" on page 14.

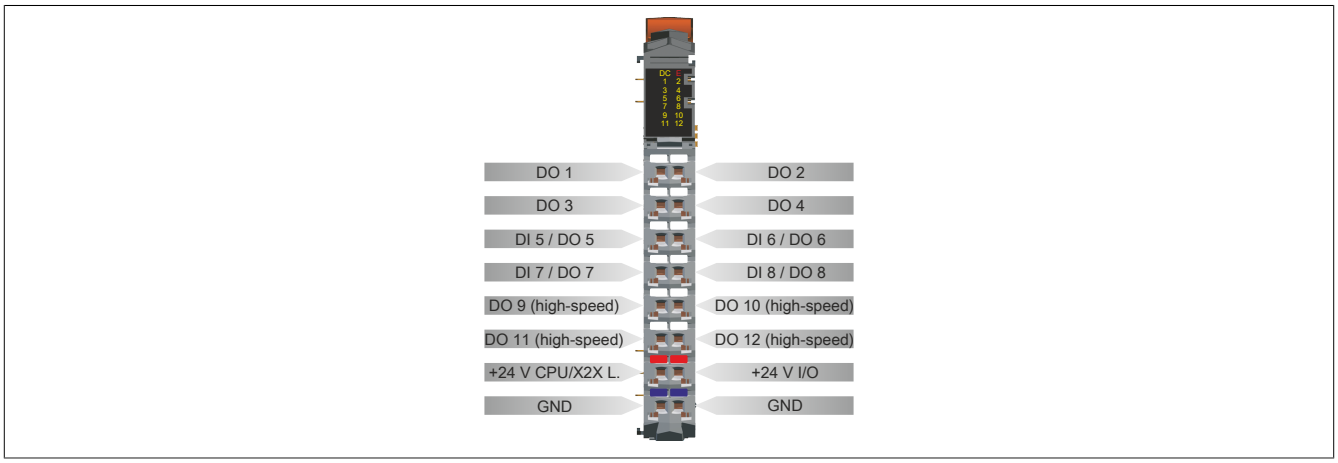


Figure 13: Pinout of the integrated X3 I/O slot

22 Connection examples

22.1 X1 I/O slot - Connection examples

Voltage/Current measurement, digital inputs and CAN bus

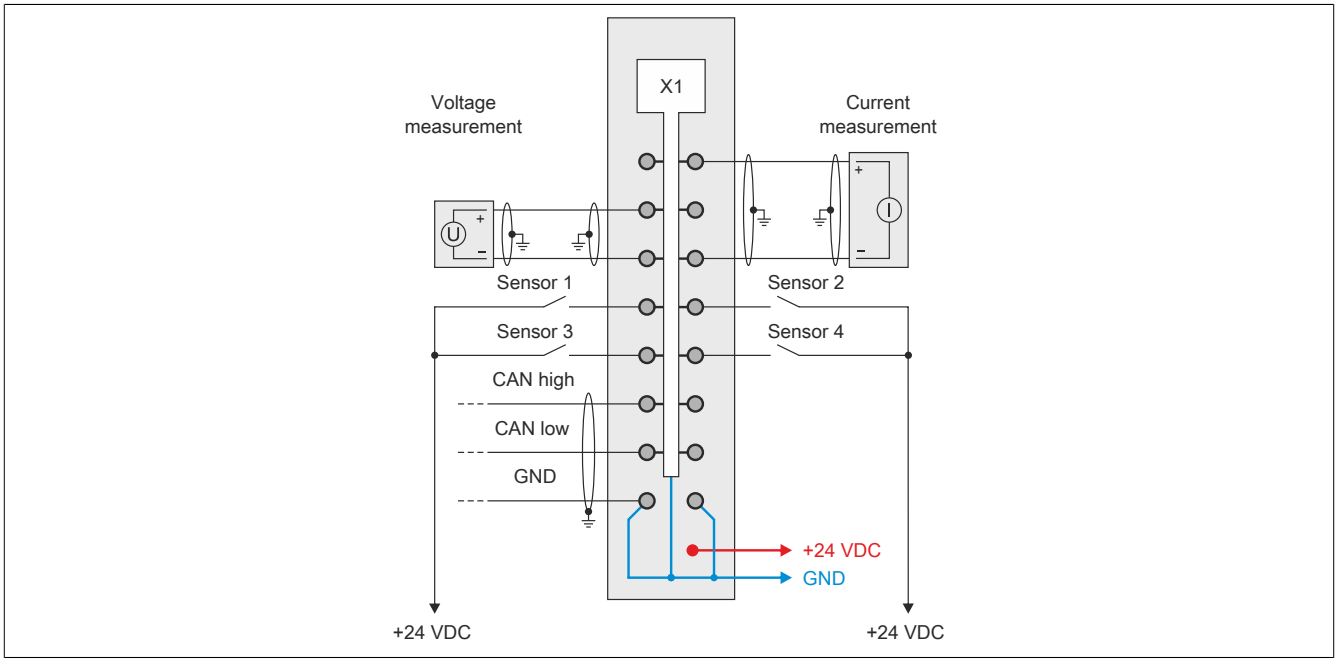


Figure 14: Connection example 1 for integrated X1 I/O slot

PT1000 resistance temperature measurement, voltage measurement, digital inputs and RS232

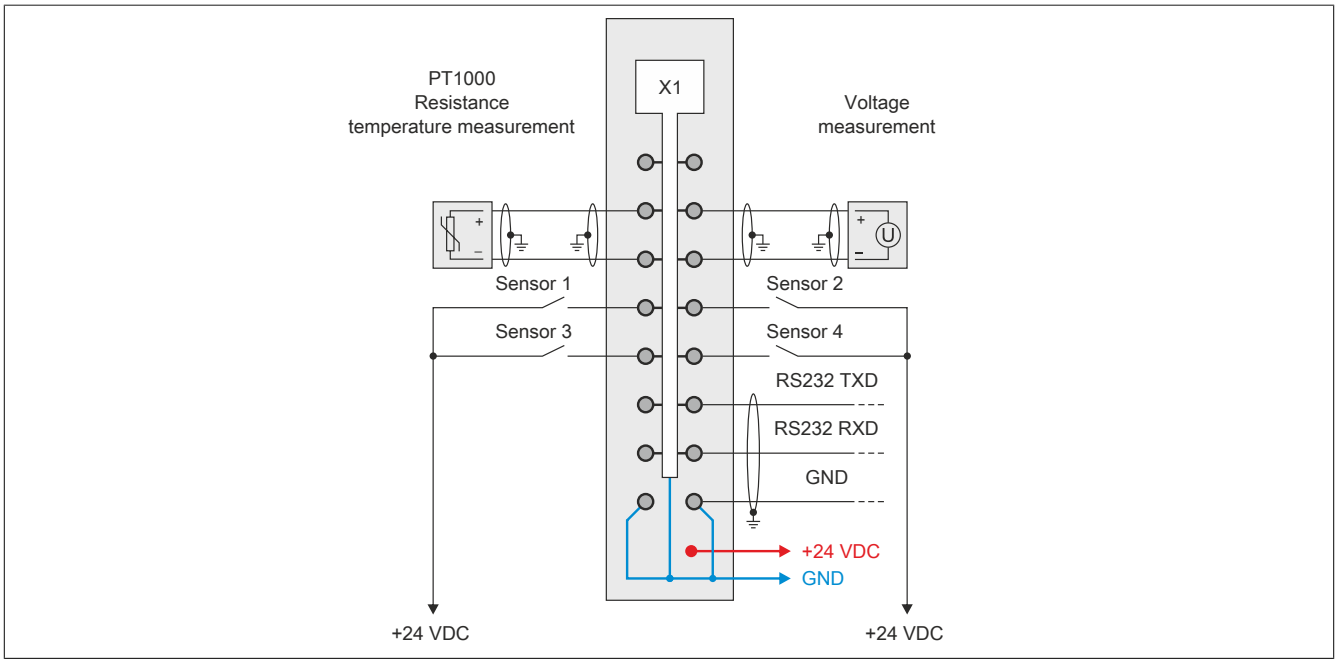


Figure 15: Connection example 2 for integrated X1 I/O slot

22.2 X2 I/O slot - Connection example

Digital inputs and ABR incremental encoder

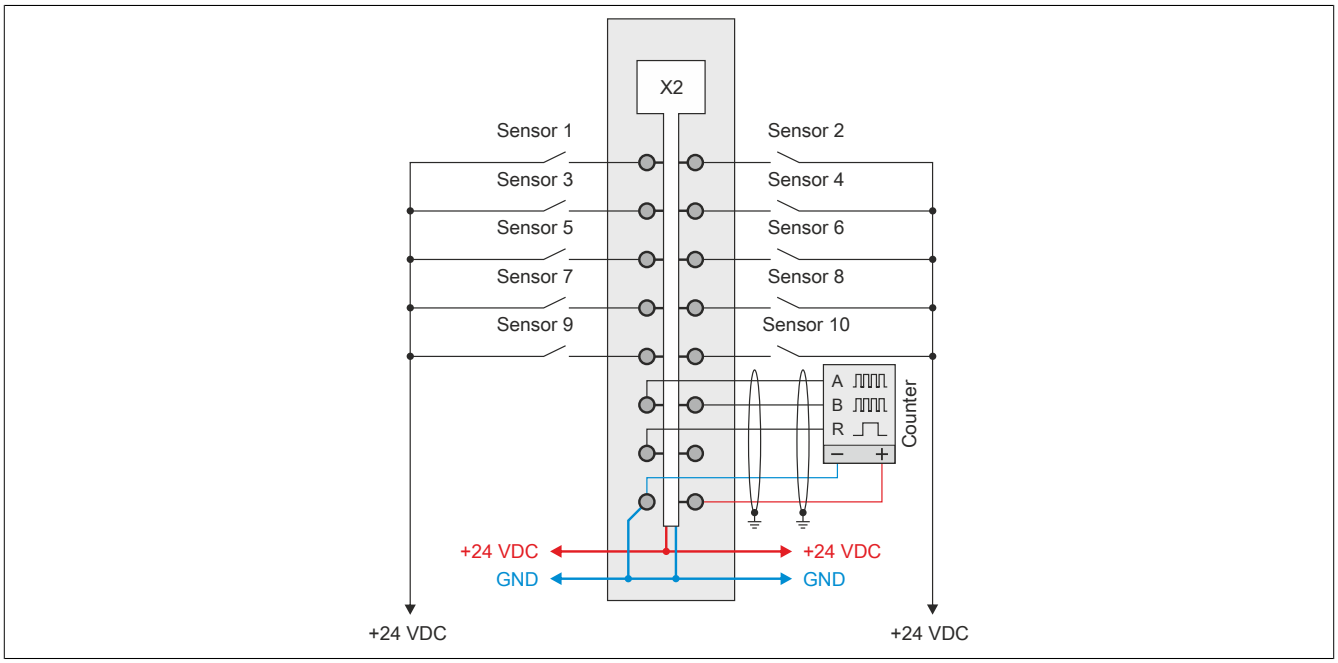


Figure 16: Connection example for integrated X2 I/O slot

22.3 X3 I/O slot - Connection example

Digital inputs/outputs, direction/frequency (DF), PWM, CPU / X2X Link supply and I/O supply

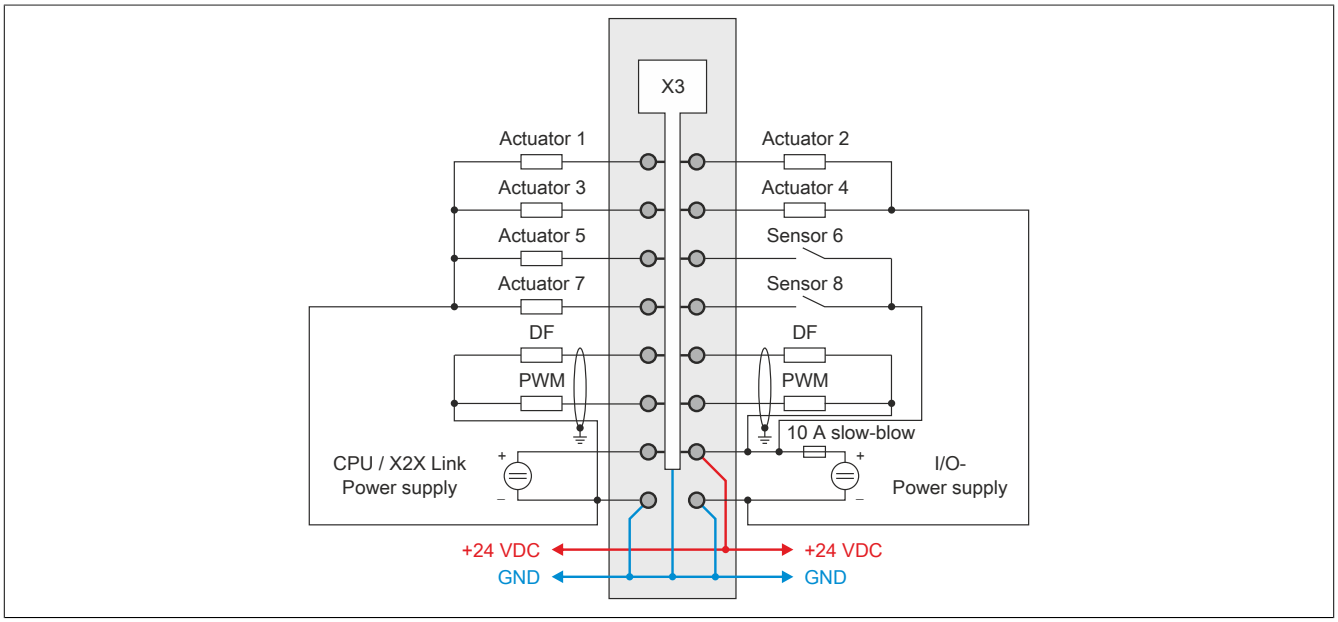


Figure 17: Connection example for integrated X3 I/O slot

23 X20 shielding bracket

The X20 shielding bracket (model number X20AC0FE1.0010) is installed below the X20 system. The shield is pressed against the shielding bracket using ground terminals from another manufacturer (e.g. PHOENIX or WAGO) or a cable tie.

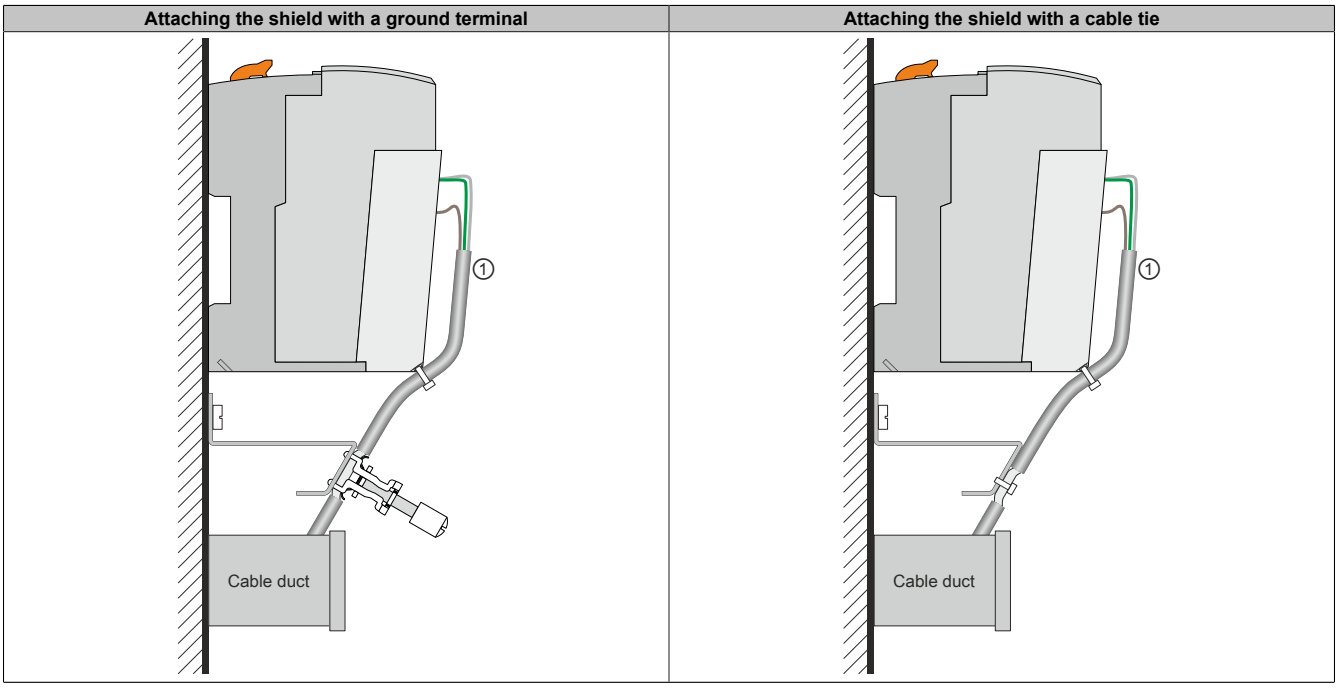


Table 18: Cable shield via X20 shielding bracket

To reduce the EMC emissions most effectively, the cable shield must reach as high as possible after the cable tie (see ① in the diagram above).

Dimensions

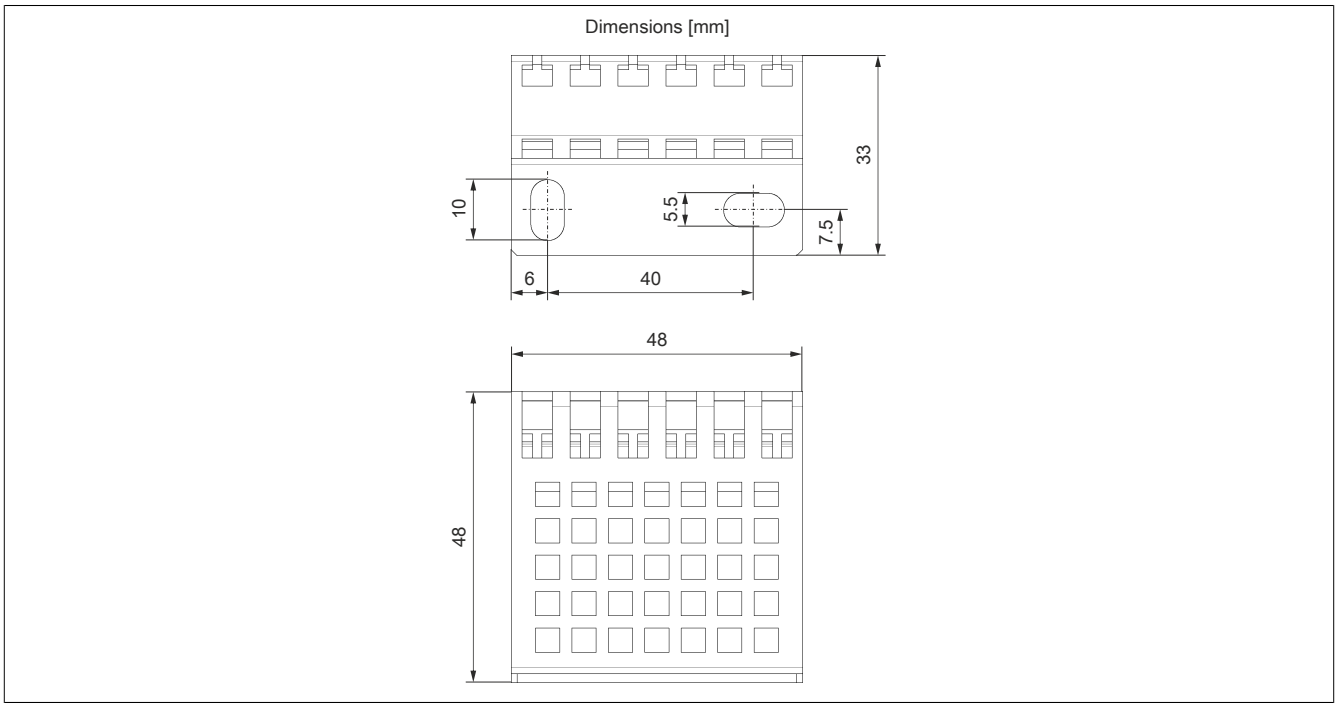


Figure 18: X20 shielding bracket - Dimensions

Content of delivery

- 10 X20 shielding brackets
- Installation template

24 Functions of the high-speed digital inputs/outputs

24.1 Functions of the high-speed digital inputs

Possible functions

The high-speed digital inputs DI 11 to DI 14 can be configured for the following functions:

Channel	Counter function				Edge detection	
DI 11	Event counter 1	A	A	D - Direction	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times
DI 12		B	B	F - Frequency	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times
DI 13	Event counter 2	A	R	R	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times
DI 14		B	E - Reference enable	E - Reference enable	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times

Table 19: Possible functions of the high-speed digital inputs DI 11 to DI 14

Please note

The following points must be taken into account to correctly configure the high-speed digital inputs:

- The counter functions are mutually exclusive. Only one type of counter function can be selected at a time. It is not possible to select two event counters (DI 11 and DI 13) at the same time together with an AB or DF counter (each on DI 13 and DI 14)!
- It is possible to select a counter function and edge detection at the same time.
- A position or counter latch is possible when configuring the high-speed inputs as a 2x event counter, ABR incremental encoder or DF function.

Examples of possible configurations

Channel	Configuration 1	Configuration 2	Configuration 3	Configuration 4
DI 11	Event counter 1	• Edge counters • Edge times	A	D
DI 12	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times	B	F
DI 13	Event counter 2	A	R	R
DI 14	• Period measurement • Gate measurement • Differential time measurement	B	E - Reference enable	E - Reference enable

Channel	Configuration 5	Configuration 6	Configuration 7	Configuration 8
DI 11	Event counter 1	A	• Period measurement • Gate measurement • Differential time measurement	D - Direction
DI 12	• Edge counters • Edge times	B	• Period measurement • Gate measurement • Differential time measurement	F - Frequency
DI 13	Event counter 2	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times	• Edge counters • Edge times
DI 14	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times	• Edge counters • Edge times	• Period measurement • Gate measurement • Differential time measurement

24.2 Functions of the high-speed digital outputs

Possible functions

The high-speed digital outputs DO 9 to DO 12 can be configured for the following functions:

Channel	Function	
DO 9	PWM - Pulse width modulation	D - Direction
DO 10	PWM - Pulse width modulation	F - Frequency
DO 11	PWM - Pulse width modulation	D - Direction
DO 12	PWM - Pulse width modulation	F - Frequency

Table 20: Possible functions of the high-speed digital inputs DO 9 to DO 12

Examples of possible configurations

Channel	Configuration 1	Configuration 2	Configuration 3	Configuration 4
DO 9	PWM - Pulse width modulation	D - Direction	PWM - Pulse width modulation	D - Direction
DO 10	PWM - Pulse width modulation	F - Frequency	PWM - Pulse width modulation	F - Frequency
DO 11	D - Direction	PWM - Pulse width modulation	PWM - Pulse width modulation	D - Direction
DO 12	F - Frequency	PWM - Pulse width modulation	PWM - Pulse width modulation	F - Frequency

25 Input/Output circuit diagram

25.1 Input circuit diagram of the analog inputs and temperature input on X1

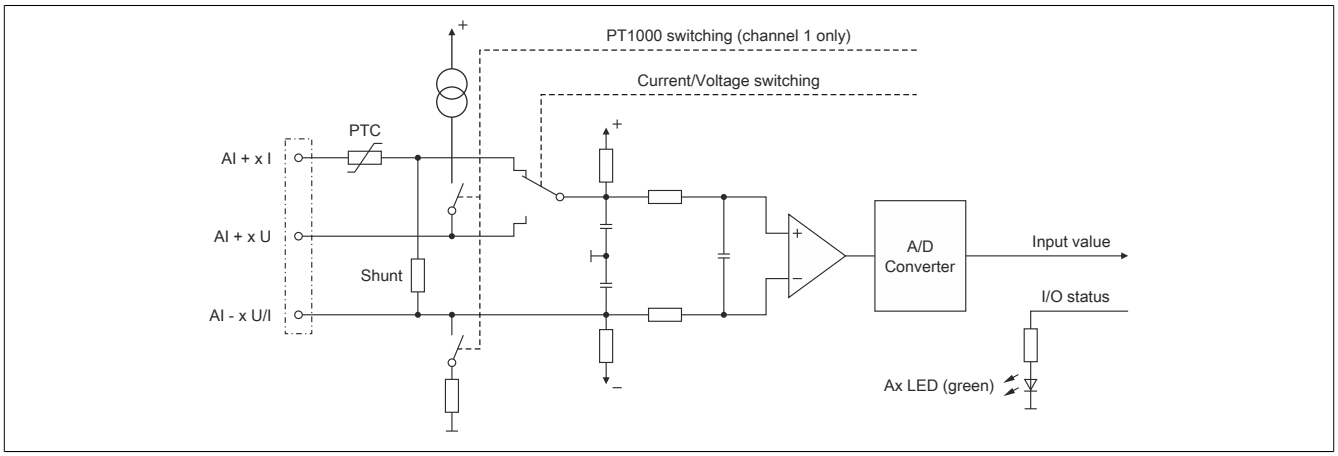


Figure 19: Input circuit diagram of the analog inputs and temperature input on the integrated X1 I/O slot

25.2 Input circuit diagram of the digital inputs

25.2.1 Input circuit diagram of the digital inputs on X1 and the high-speed digital inputs on X2

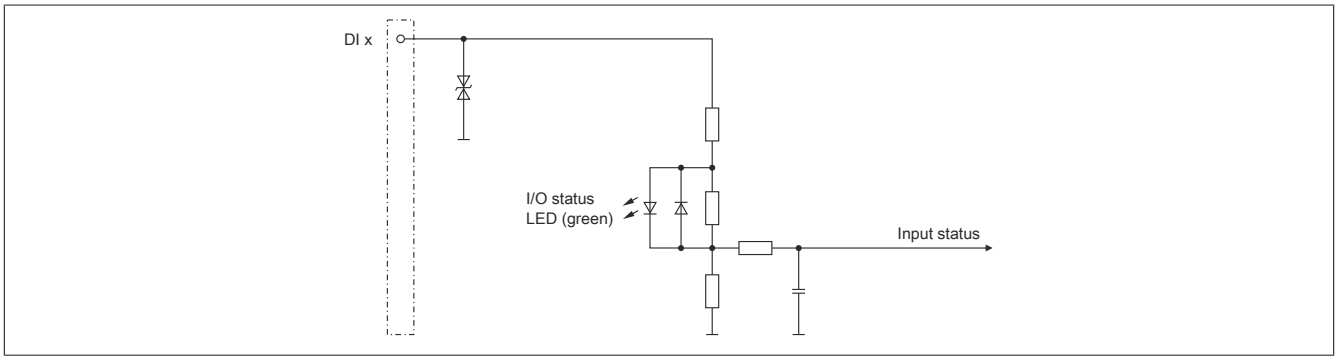


Figure 20: Input circuit diagram of the digital inputs on the integrated X1 I/O slot and the high-speed digital inputs on the integrated X2 I/O slot

25.2.2 Input circuit diagram of the digital inputs on X2

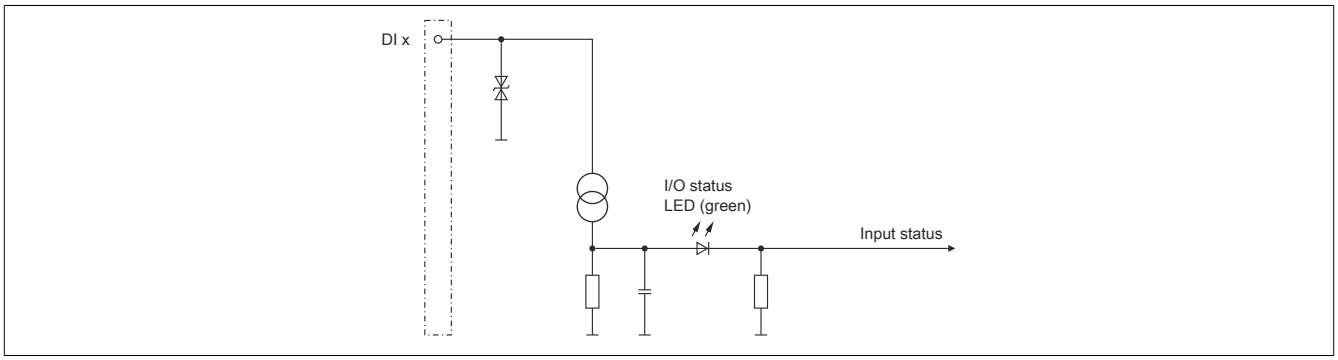


Figure 21: Input circuit diagram of the digital inputs on the integrated X2 I/O slot

25.3 Output circuit diagram of the digital outputs

25.3.1 Output circuit diagram of the digital outputs on X3

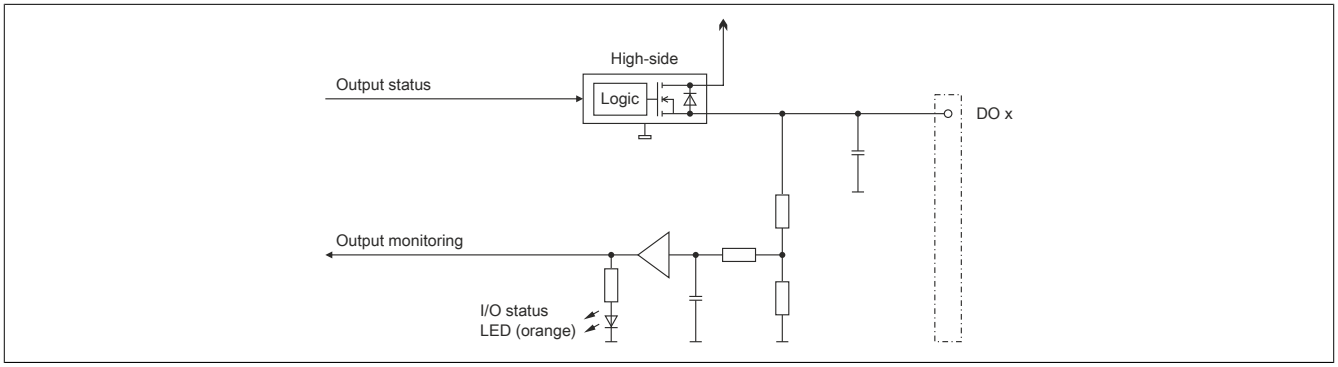


Figure 22: Output circuit diagram of the digital outputs on the integrated X3 I/O slot

25.3.2 Output circuit diagram of the high-speed digital outputs on X3

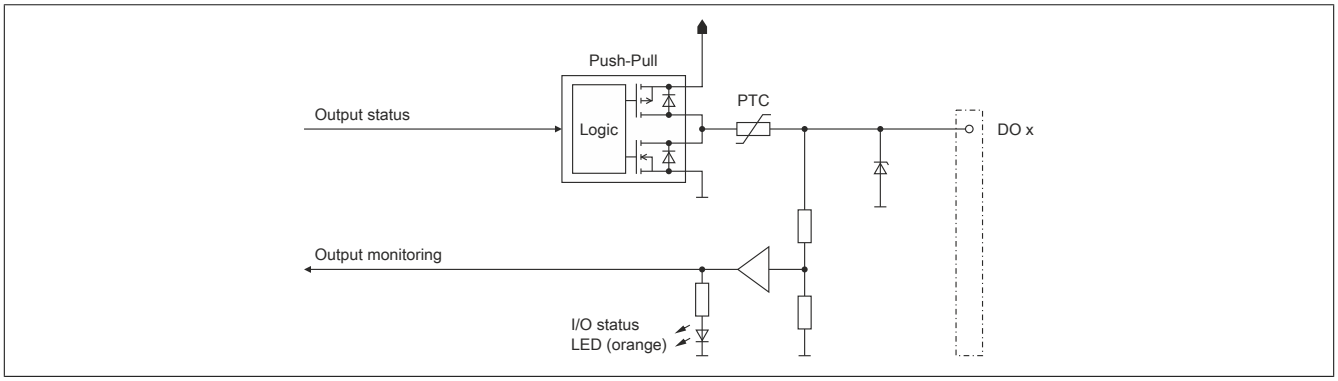


Figure 23: Output circuit diagram of the fast digital outputs on the integrated X3 I/O slot

25.4 Input/Output circuit diagram of the digital mixed channels on X3

To ensure proper operation of the digital mixed channels (DI 5 / DO 5 to DI 8 / DO 8), it is important to observe the notes in section 10.1 "Compact CPU supply concept" on page 14.

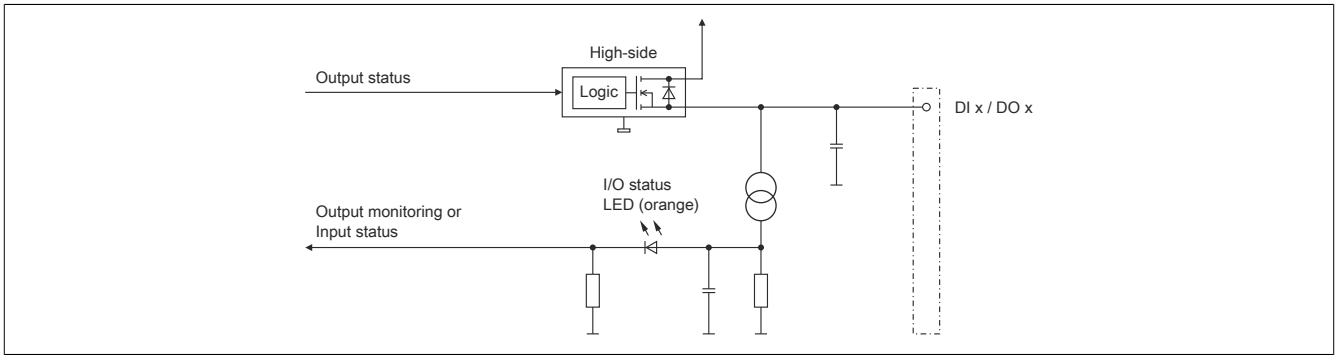


Figure 24: Input/Output circuit diagram of the digital mixed channels on the integrated X3 I/O slot

25.5 Circuit diagram for the encoder supply on X2

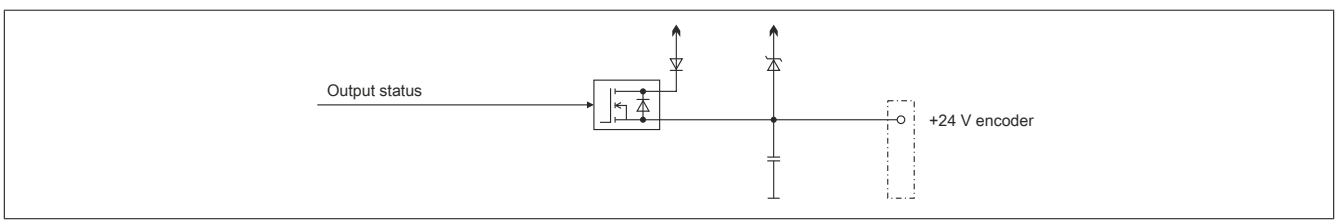


Figure 25: Circuit diagram of the encoder supply on the integrated X2 I/O slot

25.6 Circuit diagram of the CPU, X2X Link and I/O supply on X3

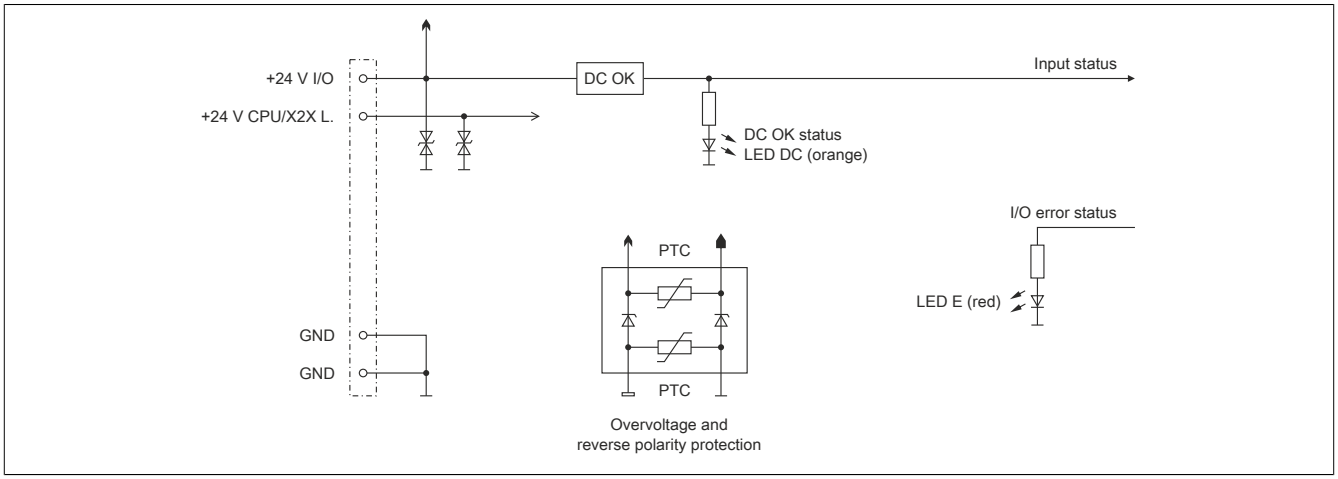


Figure 26: Circuit diagram of the CPU, X2X Link and I/O supply on the integrated X3 I/O slot

26 Switching frequency derating for high-speed digital outputs

The high-speed digital outputs can be switched with a frequency of max. 200 kHz. Derating may be necessary depending on the mounting orientation and operating temperature.

Switching frequency derating for horizontal mounting orientations

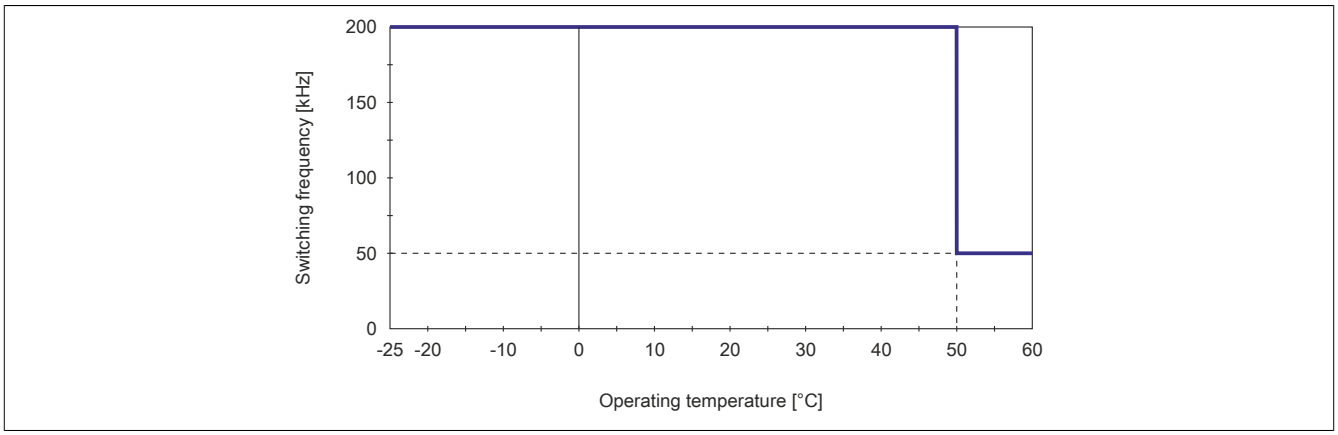


Figure 27: Switching frequency derating for high-speed digital outputs with horizontal mounting orientations

27 Register description

27.1 Register overview of the I/O data points on the integrated X1 I/O slot

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
X1 - Configuration						
2048	X1CfO_DI_Filter	USINT				•
2128	X1CfO_AI_Mode	USINT				•
2112	X1CfO_AI1_Filter	USINT				•
2116	X1CfO_AI1_LowerLim	INT				•
2118	X1CfO_AI1_UpperLim	INT				•
2120	X1CfO_AI2_Filter	USINT				•
2124	X1CfO_AI2_LowerLim	INT				•
2126	X1CfO_AI2_UpperLim	INT				•
X1 - Communication						
0	Digital inputs	USINT	•			
	DigitalInput01	Bit 0				
	DigitalInput02	Bit 1				
	DigitalInput03	Bit 2				
	DigitalInput04	Bit 3				
64	AnalogInput01	INT	•			
		UINT	•			
66	AnalogInput02	INT	•			
80	StatusInput01	USINT	•			

27.1.1 Digital inputs

Unfiltered

The input status is recorded in a 100 µs cycle.

Filtered

The filtered status is transferred in a 100 µs cycle.

Filtering takes place asynchronously in an interval of 100 µs.

27.1.1.1 Digital input filter

Name:
X1CfO_DI_Filter

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs.

Data type	Value	Filter
USINT	0	No SW filter
	1	0.1 ms
	...	...
	250	25 ms - Higher values are limited to this value

27.1.1.2 Input state of digital inputs 1 to 4

Name:
DigitalInput01 to DigitalInput04

This register is used to indicate the input state of digital inputs 1 to 4.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status of digital input 1
...		...	
3	DigitalInput04	0 or 1	Input status of digital input 4

27.1.2 Analog inputs

Analog input values are recorded in a fixed interval. The time required for conversion/updating depends on the number of analog inputs and on the input signal:

Input signal	Time required for conversion/updating
1 current/voltage input	100 µs
1 temperature/resistance input	200 µs
2 current/voltage inputs	200 µs
1 current/voltage input and 1 temperature/resistance input	400 µs

27.1.2.1 Analog input values

Name:
AnalogInput01

The analog input value is mapped to this register depending on the configured operating mode.

Data type	Value	Input signal
INT	-32,768 to 32,767	Voltage signal -10 to 10 VDC
	0 to 32,767	Current signal 0 to 20 mA (with 0 to 20 mA configuration)
	-8,192 to 32,767	Current signal 0 to 20 mA (with 4 to 20 mA configuration)
	-2,000 to 8,500	PT1000 signal -200.0 to 850.0°C
UINT	0 to 40,000	Resistance signal 0 to 4000.0 Ω

Name:
AnalogInput02

The analog input value is mapped to this register depending on the configured operating mode.

Data type	Value	Input signal
INT	-32,768 to 32,767	Voltage signal -10 to 10 VDC
	0 to 32,767	Current signal 0 to 20 mA (with 0 to 20 mA configuration)
	-8,192 to 32,767	Current signal 0 to 20 mA (with 4 to 20 mA configuration)

27.1.2.2 Input status

Name:
StatusInput01

This register holds the status of the analog inputs. A change in the monitoring status generates an error message. The following states are monitored depending on the settings:

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

Limiting the analog value

In addition to the status information, the analog value is set to the limit values listed below by default when an error occurs (see 27.1.2.5 "Limit values"). The analog value is limited to the new values if the limit values were changed.

27.1.2.3 Input filter

The analog inputs are equipped with a configurable input filter.

27.1.2.3.1 Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

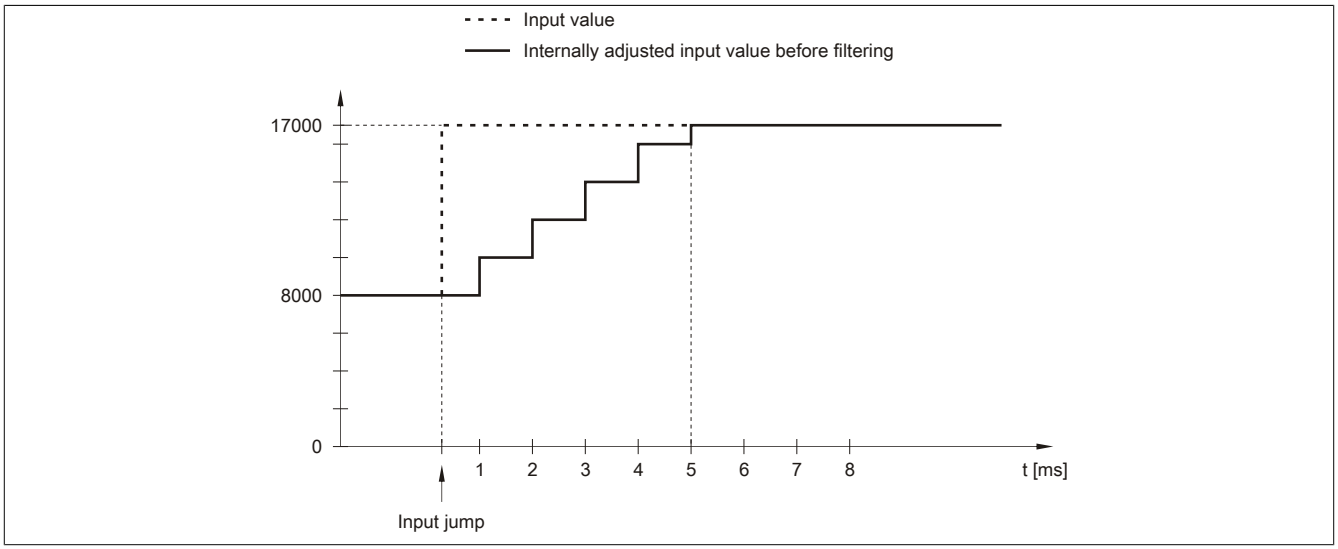


Figure 28: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

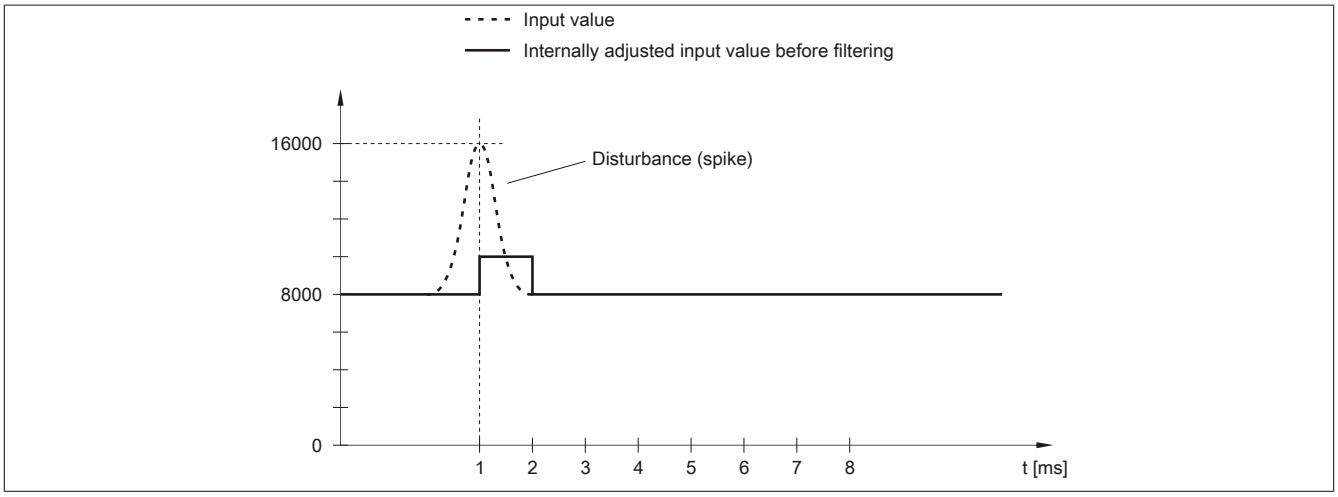


Figure 29: Adjusted input value for disturbance

27.1.2.3.2 Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{New} = Value_{Old} - \frac{Value_{Old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

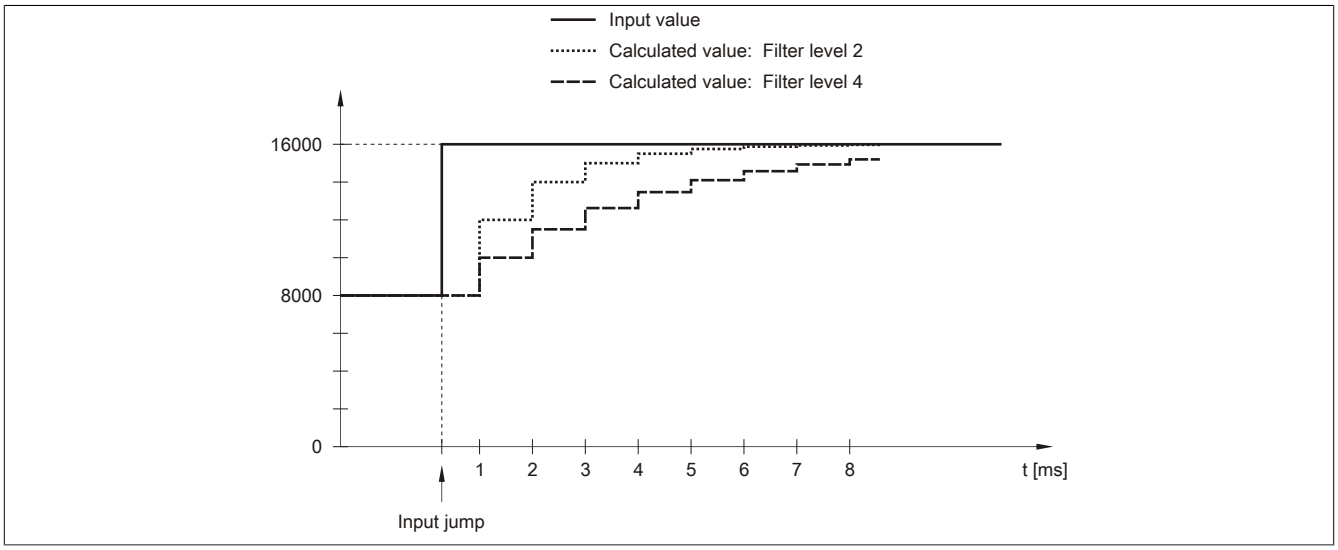


Figure 30: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

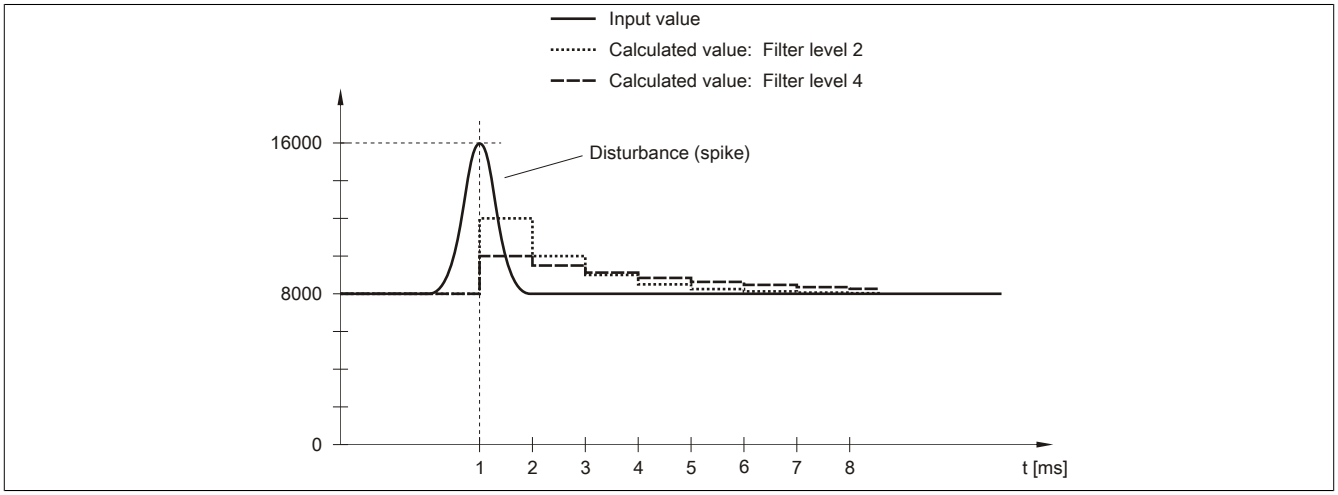


Figure 31: Calculated value during disturbance

27.1.2.3.3 Configuring the input filter

Name:
X1CfO_AI1_Filter

X1CfO_AI2_Filter

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

27.1.2.4 Channel type

Name:
X1CfO_AI_Mode

This register can be used to define the type and range of signal measurement.

Each channel is capable of handling current, voltage or resistance signals. This differentiation is made using multiple connection terminal points and an integrated switch. The switch is automatically activated depending on the specified configuration. The following input signals can be set:

Input signal	On channel
±10 V voltage signal (default)	1 and 2
0 to 20 mA current signal	1 and 2
4 to 20 mA current signal	1 and 2
PT1000 measurement	1
Resistance measurement	1

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Analog input - Channel 1	000	Channel disabled
		001	±10 V voltage signal
		010	0 to 20 mA current signal
		011	4 to 20 mA current signal
		100	PT1000 measurement
		101	Resistance measurement
3	Reserved	0	
4 - 5	Analog input - Channel 2	00	Channel disabled
		01	±10 V voltage signal
		10	0 to 20 mA current signal
		11	4 to 20 mA current signal
6 - 7	Reserved	0	

27.1.2.5 Limit values

The input signal is monitored at the upper and lower limit values. By default the following limits are set for each mode:

Limit value (default)	Voltage signal ±10 V		Current signal 0 to 20 mA		Current signal 4 to 20 mA	
Upper maximum limit value	10 V	32767 (0x7FFF)	20 mA	32767 (0x7FFF)	20 mA	32767 (0x7FFF)
Lower minimum limit value	-10 V	-32767 (0x8001)	0 mA	0[1)]	4 mA	0[2)]

Table 21: Limit values for voltage and current signals

1) The analog value is limited down to 0.
2) Due to the default limit value, the analog value is limited to a minimum of 0 at currents <4 mA.

Limit value (default)	Temperature measurement		Resistance measurement	
Upper maximum limit value	8000°C	8000 (0x1F40)	4000.0 Ω	32767 (0x7FFF)
Lower minimum limit value	-2000°C	-2000 (0xF830)	0 Ω	0

Table 22: Limit values for temperature and resistance measurement

Other limit values can be defined if necessary. These are activated automatically by writing the limit value register (see 27.1.2.5.1 "Lower limit value" and 27.1.2.5.2 "Upper limit value"). From this point on, the analog values will be monitored and limited according to the new limits. The results of monitoring are displayed in the status register (see 27.1.2.2 "Input status").

Application example of setting limit values

A negative limit value must be configured in order to measure values <4 mA with a current signal of 4 to 20 mA: 0 mA corresponds to a value of -8192 (0xE000).

27.1.2.5.1 Lower limit value

Name:
X1CfO_AI1_LowerLim
X1CfO_AI2_LowerLim

These registers can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set (see 27.1.2.2 "Input status").

Data type	Value
INT	-32,768 to 32,767
UINT	0 to 65,535

Information:

When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.

27.1.2.5.2 Upper limit value

Name:
X1CfO_AI1_UpperLim
X1CfO_AI2_UpperLim

These registers can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set (see 27.1.2.2 "Input status").

Data type	Value
INT	0 to 32,767
UINT	0 to 65,535

27.2 Register overview of the I/O data points on the integrated X2 I/O slot

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
X2 - Configuration						
7168	X2CfO_EdgeDetectUnit01Mode	USINT				●
7169	X2CfO_EdgeDetectUnit01Master	USINT				●
7170	X2CfO_EdgeDetectUnit01Slave	USINT				●
7184	X2CfO_EdgeDetectUnit02Mode	USINT				●
7185	X2CfO_EdgeDetectUnit02Master	USINT				●
7186	X2CfO_EdgeDetectUnit02Slave	USINT				●
6144	X2CfO_DI_Filter	USINT				●
6528	X2CfO_CounterMode	USINT				●
6400	X2CfO_Latch01Mode	USINT				●
6401	X2CfO_Latch01Comparator	USINT				●
6416	X2CfO_Latch02Mode	USINT				●
6417	X2CfO_Latch02Comparator	USINT				●
X2 - Communication						
4096	Digital inputs	USINT	●			
	DigitalInput01	Bit 0				
	DigitalInput02	Bit 1				
	DigitalInput03	Bit 2				
	DigitalInput04	Bit 3				
	DigitalInput05	Bit 4				
	DigitalInput06	Bit 5				
	DigitalInput07	Bit 6				
	DigitalInput08	Bit 7				
4097	Digital inputs	USINT	●			
	DigitalInput09	Bit 0				
	DigitalInput10	Bit 1				
	DigitalInput11	Bit 2				
	DigitalInput12	Bit 3				
	DigitalInput13	Bit 4				
	DigitalInput14	Bit 5				
5120	EdgeDetect01Mastertime	DINT	●			
5124	EdgeDetect01Difference	DINT	●			
5128	EdgeDetect01Mastercount	INT	●			
5136	EdgeDetect02Mastertime	DINT	●			
5140	EdgeDetect02Difference	DINT	●			
5144	EdgeDetect02Mastercount	INT	●			
4384	Counter 1	USINT			●	
	Counter01Reset	Bit 0				
	Latch01Enable	Bit 1				
4352	Counter01Value	DINT	●			
4356	Counter01Latch	DINT	●			
4360	Counter01TimeChanged	DINT	●			
4364	Counter01TimeValid	DINT	●			
4368	Latch01Count	SINT	●			
4448	Counter 2	USINT			●	
	Counter02Reset	Bit 0				
	Latch02Enable	Bit 1				
4416	Counter02Value	DINT	●			
4420	Counter02Latch	DINT	●			
4424	Counter02TimeChanged	DINT	●			
4428	Counter02TimeValid	DINT	●			
4432	Latch02Count	SINT	●			

27.2.1 Digital inputs

Unfiltered

The input status is recorded in a 100 µs cycle.

Filtered

The filtered status is transferred in a 100 µs cycle.

Filtering takes place asynchronously in an interval of 100 µs.

27.2.1.1 Digital input filter

Name:
X2CfO_DI_Filter

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs.

Data type	Value	Filter
USINT	0	No SW filter
	1	0.1 ms
	...	...
	250	25 ms - Higher values are limited to this value

27.2.1.2 Input state of digital inputs 1 to 14

Name:
DigitalInput01 to DigitalInput14

These registers are used to indicate the input state of digital inputs 1 to 14.

Data type	Value
USINT	See bit structure.

Bit structure of register 4096:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status of digital input 1
...		...	
7	DigitalInput08	0 or 1	Input status of digital input 8

Bit structure of register 4097:

Bit	Name	Value	Information
0	DigitalInput09	0 or 1	Input status of digital input 9
...		...	
5	DigitalInput14	0 or 1	Input status of digital input 14

27.2.2 Edge detection

Digital inputs 11 to 14 can be used for fast edge detection. This runs parallel to all other functions such as counters, etc. This function does not use the digital input filter.

The edge detection function measures edges with µs precision. 2 units are available. A master and a slave edge can be configured for each unit. At each master edge, the timestamp of the master edge and the differential time to the previous slave edge (if present) are logged. A "Master count" can always be utilized to determine how many edges have been detected since the last task class cycle. The timestamp is based on the system time of the CPU.

The combination of rising/falling edges of each channel can be used to configure the following functions for each unit:

Function	Description
Edge time	Measure an edge time
Period duration	Measure the master and differential time
Gate time	Measure the master and differential time
Time offset	Measure the master and differential time of edges on different channels

27.2.2.1 Edge detection unit - Mode settings

The edge detection unit needs to be configured according to the desired function.

Function	Description
Basic timestamp, master edge mode	The current system time is saved as the master time at the time of the edge.
Timestamp and/or differential time, master and slave edge mode	The slave edge starts the measurement and the system time is saved temporarily. When the master edge occurs, the current system time is saved as the master time and the difference between the master and slave edges is calculated.

Name:
X2CfO_EdgeDetectUnit01Mode
X2CfO_EdgeDetectUnit02Mode

These registers are used to configure the mode of the basic function for either just the master edge or both master and slave edges.

Data type	Value	Information
USINT	0x00	Edge detection disabled on Unit0x: Time measurement not possible
	0x80	Edge detection enabled on Unit0x: Reaction only possible for master edge, no differential measurement possible
	0xC0	Edge detection enabled on Unit0x: Reaction possible for configured master and slave edges

27.2.2.2 Edge detection unit - Selection of master edge

Name:
X2CfO_EdgeDetectUnit01Master
X2CfO_EdgeDetectUnit02Master

These registers are used to select the source of the master edge for the respective unit. Either the rising or falling edge of one of the 4 fast digital input channels can be selected. Only one edge can be selected for each unit.

Data type	Value	Information
USINT	0	Digital input channel 11: Rising edge
	2	Digital input channel 12: Rising edge
	4	Digital input channel 13: Rising edge
	6	Digital input channel 14: Rising edge
	1	Digital input channel 11: Falling edge
	3	Digital input channel 12: Falling edge
	5	Digital input channel 13: Falling edge
	7	Digital input channel 14: Falling edge

27.2.2.3 Edge detection unit - Selection of slave edge

Name:
X2CfO_EdgeDetectUnit01Slave
X2CfO_EdgeDetectUnit02Slave

These registers are used to select the source of the slave edge for the respective unit. Either the rising or falling edge of one of the 4 fast digital input channels can be selected. Only one edge can be selected for each unit.

Data type	Value	Information
USINT	0	Digital input channel 11: Rising edge
	2	Digital input channel 12: Rising edge
	4	Digital input channel 13: Rising edge
	6	Digital input channel 14: Rising edge
	1	Digital input channel 11: Falling edge
	3	Digital input channel 12: Falling edge
	5	Digital input channel 13: Falling edge
	7	Digital input channel 14: Falling edge

27.2.2.4 Edge detection unit - Master edge counter

Name:
EdgeDetect01Mastercount
EdgeDetect02Mastercount

These registers hold the counter values of the detected master edges. The counter value is used to detect new measurements.

Data type	Value	Information
INT	-32,768 to 32,767	Running counter: Number of detected master edges

27.2.2.5 Edge detection unit - Master edge timestamp

Name:
EdgeDetect01Mastertime
EdgeDetect02Mastertime

The exact CPU system time of the respective unit is saved to these registers when a master edge occurs. If multiple master edges occur within a single cycle (task class), then the time of the last edge is shown.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	CPU system time of master edge [µs]

27.2.2.6 Edge detection unit - Time difference

Name:
EdgeDetect01Difference
EdgeDetect02Difference

The difference between the master edge and the slave edge of the respective unit is saved to these registers. If multiple measurement periods are completed within a single cycle (task class), then the time difference from the last period is shown.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Time difference between master edge and slave edge [µs]

27.2.3 Counter functions

Fast digital inputs 11 to 14 can be used for counter functions. This function does not use the digital input filter. The following functions are available. Only one of these basic configurations can be enabled at a time:

- 2x event counter with latch function
- 2x AB incremental counter without latch function
- DF counter function
- ABR counter function

27.2.3.1 Configuring the counter function

The following counter functions can be configured:

Counter function	Description
2x event counter with latch function	Input 11 for event counter 1 and input 13 for event counter 2 can be used simultaneously as event counters. Both rising and falling edges are counted. The latch function of all 4 inputs can be used.
2x AB incremental counter without latch function	Inputs 11 and 12 as AB counter 1 and inputs 13 and 14 as AB counter 2. Since no more fast inputs are available, the latch function is not available.
DF counter: Direction/Frequency with latch function	The D, F and R signals are linked to inputs 11, 12 and 13. Signal D defines the positive (Level = 0) or negative (Level = 1) counting direction. The latch function of all 4 inputs can be used.
ABR counter with latch function	The A, B and R signals are linked to inputs 11, 12 and 13. The latch function of all 4 inputs can be used.

Name:
X2CfO_CounterMode

This register configures the counter function:

Data type	Value	Information
USINT	0	2x event counter with latch function
	1	2x AB incremental counter without latch function
	2	DF counter with latch function
	3	ABR counter with latch function

27.2.3.2 Configuring the mode of the latch function

Name:
X2CfO_Latch01Mode
X2CfO_Latch02Mode

This register sets the mode of the latch function. The following latch functions can be configured:

Latch function	Description
Single shot latch mode	The latch function must be enabled/set. After a successful latch procedure the function must first be reset. Then it can be enabled again.
Continuous latch mode	The latch function only has to be enabled/set as long as latching is desired.

A changed counter value on "LatchCount" indicates that the latch procedure has been performed (see 27.2.3.7 "Counter value of latch events"). The counter value is stored in the latch register (see 27.2.3.6 "Latched counter value").

Data type	Value	Information
USINT	0	Single shot latch mode
	1	Continuous latch mode

27.2.3.3 Configuring the latch signals

Name:
X2CfO_Latch01Comparator
X2CfO_Latch02Comparator

This register defines the inputs and their level for triggering the latch procedure.

- This defines which inputs are linked to generate the latch event. All 4 digital input signals can be used for an "AND" connection.
- The "active voltage level" needed for the latch procedure can be defined to adjust for the physical signals. It is not possible to configure a high and low level at the same time.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Value	Information
0	0	Input 11 high level disabled
	1	Input 11 high level enabled for comparator
1	0	Input 12 high level disabled
	1	Input 12 high level enabled for comparator
2	0	Input 13 high level disabled
	1	Input 13 high level enabled for comparator
3	0	Input 14 high level disabled
	1	Input 14 high level enabled for comparator
4	0	Input 11 low level disabled
	1	Input 11 low level enabled for comparator
5	0	Input 12 low level disabled
	1	Input 12 low level enabled for comparator
6	0	Input 13 low level disabled
	1	Input 13 low level enabled for comparator
7	0	Input 14 low level disabled
	1	Input 14 low level enabled for comparator

27.2.3.4 Clear counter value and enable/disable latch function

Name:
Counter01Reset
Counter02Reset
Latch01Enable
Latch02Enable

The respective bits in these registers clear the counter value or start the latch procedure.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Counter0xReset	0	Do not reset the counter
		1	Reset the counter
1	Latch0xEnable	0	Do not latch the counter
		1	Latch the counter
2 - 7	Reserved	0	

27.2.3.5 Counter value

Name:
Counter01Value
Counter02Value

The current counter values are saved in these registers.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Current counter value

27.2.3.6 Latched counter value

Name:
Counter01Latch
Counter02Latch

As soon as the latch conditions have been met, the value of the respective counter is copied to these registers.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Latched counter value

27.2.3.7 Counter value of latch events

Name:
Latch01Count
Latch02Count

These registers hold the counter values of the latch events. This allows detection of whether a new latched counter value has been saved.

Data type	Value	Information
DINT	-128 to 127	Running counter: Number of detected latch events

27.2.3.8 Timestamp of last counter change

Name:
Counter01TimeChanged
Counter02TimeChanged

The CPU system time at the time of the last change to the counter value is saved in these registers.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	The CPU system time at the time of the last change to the counter value

27.2.3.9 Timestamp of last valid counter value

Name:
Counter01TimeValid
Counter02TimeValid

The CPU system time at the time of the last valid counter value is saved in these registers.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	CPU system time of current counter value

27.3 Register overview of the I/O data points on the integrated X3 I/O slot

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
X3 - Configuration						
10240	X3CfO_DI_Filter	USINT				•
10752	X3CfO_Mov01Mode	USINT				•
10756	X3CfO_Mov01SpeedLimit	UDINT				•
10768	X3CfO_Mov02Mode	USINT				•
10772	X3CfO_Mov02SpeedLimit	UDINT				•
12032	X3CfO_PhyIOConfigCh01	USINT				•
12033	X3CfO_PhyIOConfigCh02	USINT				•
12034	X3CfO_PhyIOConfigCh03	USINT				•
12035	X3CfO_PhyIOConfigCh04	USINT				•
12036	X3CfO_PhyIOConfigCh05	USINT				•
12037	X3CfO_PhyIOConfigCh06	USINT				•
12038	X3CfO_PhyIOConfigCh07	USINT				•
12039	X3CfO_PhyIOConfigCh08	USINT				•
12040	X3CfO_PhyIOConfigCh09	USINT				•
12041	X3CfO_PhyIOConfigCh10	USINT				•
12042	X3CfO_PhyIOConfigCh11	USINT				•
12043	X3CfO_PhyIOConfigCh12	USINT				•
X3 - Communication						
8192	Digital inputs	USINT	•			
	DigitalInput05	Bit 0				
	DigitalInput06	Bit 1				
	DigitalInput07	Bit 2				
	DigitalInput08	Bit 3				
8208	Digital outputs	USINT			•	
	DigitalOutput01	Bit 0				
	DigitalOutput02	Bit 1				
	DigitalOutput03	Bit 2				
	DigitalOutput04	Bit 3				
	DigitalOutput05	Bit 4				
	DigitalOutput06	Bit 5				
	DigitalOutput07	Bit 6				
	DigitalOutput08	Bit 7				
8209	Digital outputs	USINT			•	
	DigitalOutput09	Bit 0				
	DigitalOutput10	Bit 1				
	DigitalOutput11	Bit 2				
	DigitalOutput12	Bit 3				
8193	Status feedback	USINT	•			
	StatusDigitalOutput01	Bit 0				
	StatusDigitalOutput02	Bit 1				
	StatusDigitalOutput03	Bit 2				
	StatusDigitalOutput04	Bit 3				
	StatusDigitalOutput05	Bit 4				
	StatusDigitalOutput06	Bit 5				
	StatusDigitalOutput07	Bit 6				
	StatusDigitalOutput08	Bit 7				
8194	Status feedback	USINT	•			
	StatusDigitalOutput09	Bit 0				
	StatusDigitalOutput10	Bit 1				
	StatusDigitalOutput11	Bit 2				
	StatusDigitalOutput12	Bit 3				
4864	PWMPeriod09	UINT			•	
4866	PWMOutput09	INT			•	
4880	PWMPeriod10	UINT			•	
4882	PWMOutput10	INT			•	
4896	PWMPeriod11	UINT			•	
4898	PWMOutput11	INT			•	
4912	PWMPeriod12	UINT			•	
4914	PWMOutput12	INT			•	
8704	Movement 1	USINT			•	
	Mov01Enable	Bit 1				
8706	Mov01Speed	INT			•	
8708	Mov01Position	DINT	•			
8720	Movement 2	USINT			•	
	Mov02Enable	Bit 2				
8722	Mov02Speed	INT			•	
8724	Mov02Position	DINT	•			
8196	StatusInput01	BOOL	•			

27.3.1 Physical configuration of I/O channels

These registers are used to define the functionality of the channels. Depending on the desired configuration, the following assignments can be made with respect to the existing software and hardware:

- A physical configuration as input or output for mixed channels
- An explicit assignment as direct I/O channel: i.e. digital input or digital output
- An explicit assignment as PWM output
- An explicit assignment as D or F movement output

27.3.1.1 Physical configuration

Name:
X3CfO_PhyIOConfigCh01 to X3CfO_PhyIOConfigCh12

These registers are used to configure the functionality of the channels.

Data type	Value
USINT	See bit structure.

Bit structure:

Name:
X3CfO_PhyIOConfigCh01 to X3CfO_PhyIOConfigCh04

Channels 1 to 4 are digital outputs and can only be used as direct I/O channel.

Bit	Description	Value	Information
0 - 7		0	Direct I/O operation of output

Name:
X3CfO_PhyIOConfigCh05 to X3CfO_PhyIOConfigCh08

Channels 5 to 8 are digital mixed channels and can be configured as either input or output.

Bit	Description	Value	Information
0 - 1		00	Configured as digital output
		01	Reserved
		10	Reserved
		11	Configured as digital input
2 - 7		0	Direct I/O operation of output

Name:
X3CfO_PhyIOConfigCh09 to X3CfO_PhyIOConfigCh12

Channels 9 to 12 are fast digital outputs and can be configured as direct I/O, PWM or movement channels.

Bit	Description	Value	Information
0 - 3	Reserved	0	
4 - 5		00	Direct I/O operation of output
		01	Output operated as PWM
		10	Reserved
		11	Output operated as D/F movement
6 - 7	Reserved	0	

27.3.2 Monitoring of the I/O supply voltage

Name:
StatusInput01

The status of the I/O supply voltage is shown in this register.

Data type	Value	Information
USINT	0	I/O supply voltage within permitted range
	1	I/O supply voltage not connected or outside of the permitted range

27.3.3 Digital inputs

Unfiltered

The input status is recorded in a 100 µs cycle.

Filtered

The filtered status is transferred in a 100 µs cycle.

Filtering takes place asynchronously in an interval of 100 µs.

27.3.3.1 Digital input filter

Name:
X3CfO_DI_Filter

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs.

Data type	Value	Filter
USINT	0	No SW filter
	1	0.1 ms
	...	...
	250	25 ms - Higher values are limited to this value

27.3.3.2 Input state of digital inputs 5 to 8

Name:
DigitalInput05 to DigitalInput08

This register is used to indicate the input state of digital inputs 5 to 8.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput05	0 or 1	Input status of digital input 5
...		...	
3	DigitalInput08	0 or 1	Input status of digital input 8

27.3.4 Digital outputs

The output status is processed in a 100 µs cycle.

27.3.4.1 Switching state of digital outputs 1 to 12

Name:
DigitalOutput01 to DigitalOutput12

These registers are used to store the switching state of digital outputs 1 to 12.

Data type	Value
USINT	See bit structure.

Bit structure:

Register 8208:

Bit	Description	Value	Information
0	DigitalOutput01	0	Digital output 1 reset
		1	Digital output 1 set
...		...	
7	DigitalOutput08	0	Digital output 8 reset
		1	Digital output 8 set

Register 8209:

Bit	Description	Value	Information
0	DigitalOutput09	0	Digital output 9 reset
		1	Digital output 9 set
...		...	
3	DigitalOutput12	0	Digital output 12 reset
		1	Digital output 12 set

27.3.5 Monitoring status of the digital outputs

The error states of the outputs must be programmed in the application. The status information that is read is the actual voltage state on the channel (set or reset). The error state is therefore determined by a difference between the data points "DigitalOutputxx" and the corresponding "StatusDigitalOutputxx".

At least 3 system ticks are needed internally to read the output status. This is the reason for the delay after which the earliest possible comparison can be made after a change in the status of the output.

The digital input filter is not applied to this status information.

27.3.5.1 Status of digital outputs 1 to 12

Name:
StatusDigitalOutput01 to StatusDigitalOutput12

These registers are used to indicate the status of digital outputs 1 to 12.

Data type	Value
USINT	See bit structure.

Bit structure:

Register 8193:

Bit	Description	Value	Information
0	StatusDigitalOutput01	0	Channel 1: Digital output reset or short circuit
		1	Channel 1: Digital output set or voltage feedback
...		...	
7	StatusDigitalOutput08	0	Channel 8: Digital output reset or short circuit
		1	Channel 8: Digital output set or voltage feedback

Register 8194:

Bit	Description	Value	Information
0	StatusDigitalOutput09	0	Channel 9: Digital output reset or short circuit
		1	Channel 9: Digital output set or voltage feedback
...		...	
3	StatusDigitalOutput12	0	Channel 12: Digital output reset or short circuit
		1	Channel 12: Digital output set or voltage feedback

27.3.6 Pulse width modulation (PWM) function

Digital inputs 9 to 12 can be configured as PWM outputs. Two data points are available per channel for controlling the PWM signal.

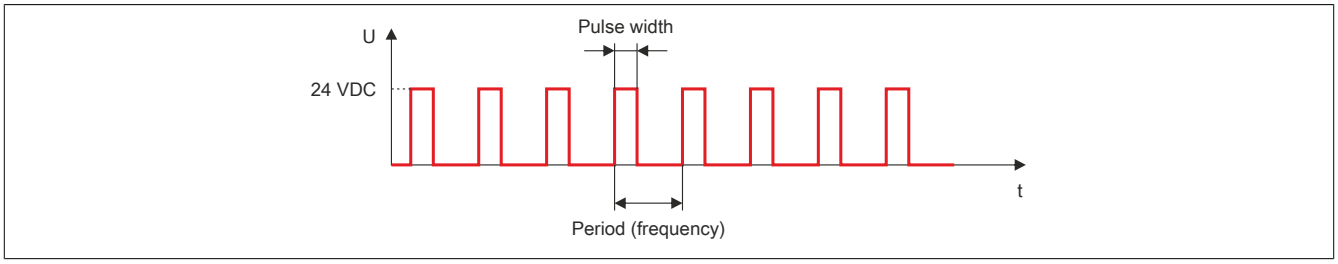


Figure 32: The PWM signal is controlled by setting the pulse width and the duration of the period

27.3.6.1 Period duration of the PWM outputs

Name:
PWMPeriod09 to PWMPeriod12

These registers are used to define the duration of the period, i.e. the time base for the respective PWM output. This time represents the 100% value, which can be resolved to 0.1% through the duty cycle.

Data type	Value	Information
UINT	5 to 65,535	Duration of period, between 5 and 65535 µs: Corresponds to a frequency between 200 kHz and ~15 Hz

27.3.6.2 Duty cycle of the PWM outputs

Name:
PWMOutput09 to PWMOutput12

These registers output the duty cycle of the respective PWM output in a resolution of 0.1% of the period.

Data type	Value	Information
INT	0 to 1,000	Duty cycle of the output in 0 to 100.0%

Example: Period duration T [µs] with a duty cycle of 25% equals a duty time of t_1 [µs].

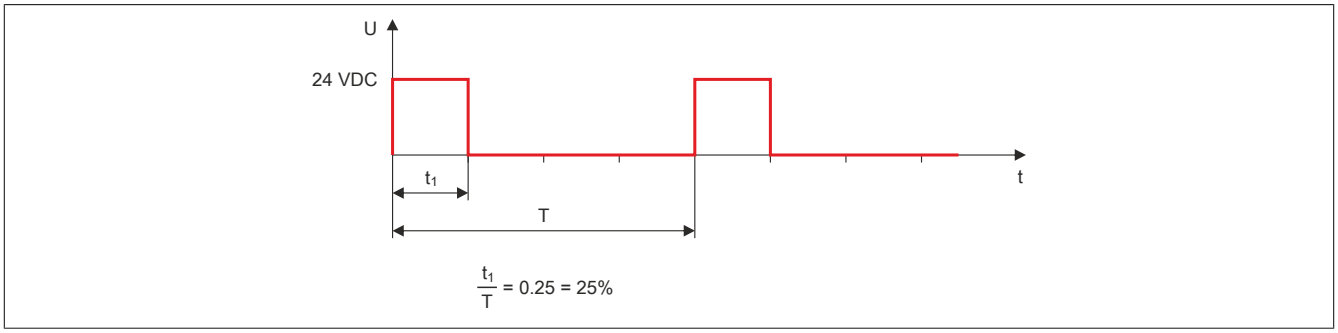


Figure 33: Duty time as a function of the period and the duty cycle

27.3.7 DF movement generator function

Digital output channels 9 to 12 can be configured as 2 independently functioning movement generators (Direction/Frequency) for stepper motor control. The movement generators are assigned to the following channels:

Movement generator	Channel	Function
1	DO 9	D: Direction
	DO 10	Q: Frequency
2	DO 11	D: Direction
	DO 12	Q: Frequency

The frequency is output via the respective F channel, and the direction is output via the respective D channel. The switchover between directions (movement/counter) takes place via the sign of the speed setpoint.

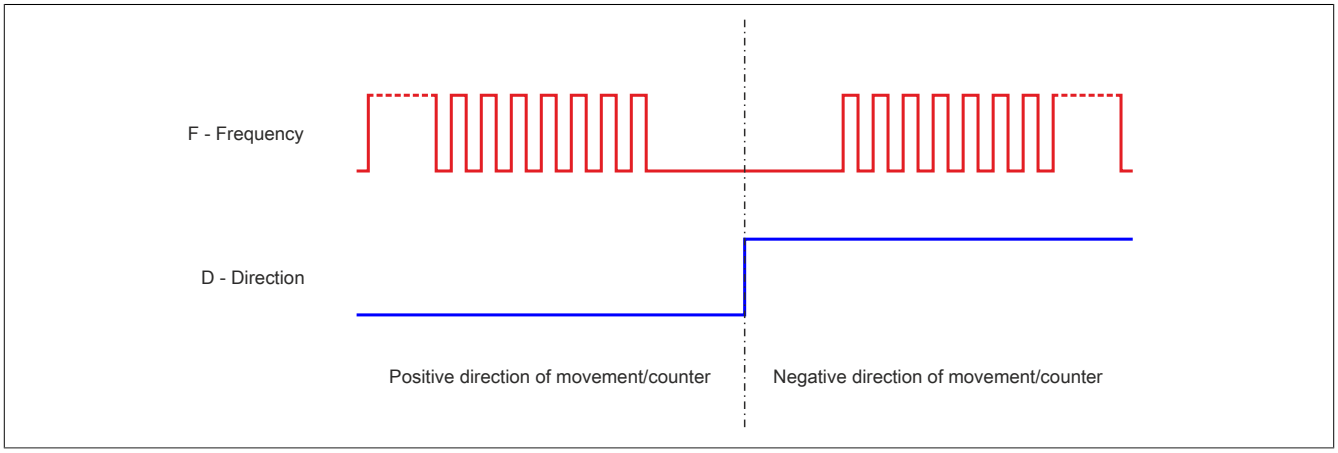


Figure 34: Frequency output via F channel, direction output via D channel

The respective output must be configured correctly in order to completely process the movement function (see 27.3.1.1 "Physical configuration").

The data points described below are available for configuring and controlling the respective movements.

27.3.7.1 Configuring the movement mode

Name:
X3Cfo_Mov01Mode
X3Cfo_Mov02Mode

These registers are used to configure how the speed setpoint is interpreted. The difference between the two modes is whether edges or periods are output for each increment of the setpoint.

Data type	Value	Information
USINT	0	Edge mode: Each increment generates an edge on the output
	1	Pulse mode: Each increment generates a period on the output

Edge mode

4 increments of the speed setpoint correspond to 2 periods on the output:

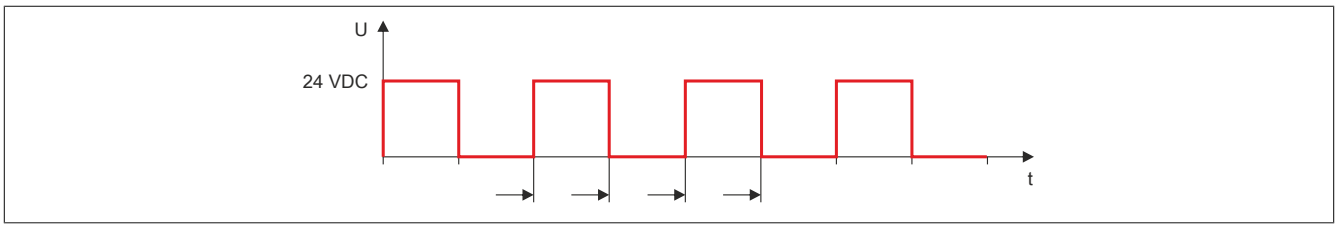


Figure 35: Interpretation of the speed setpoint with edge output for each increment

Pulse mode

2 increments of the speed setpoint correspond to 2 periods on the output:

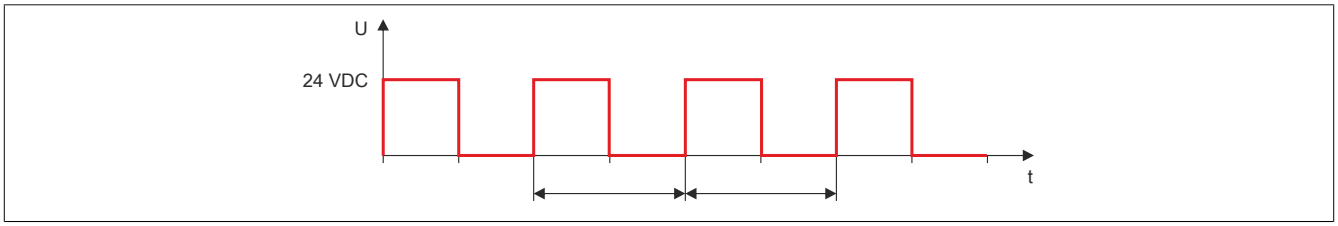


Figure 36: Interpretation of the speed setpoint with period output for each increment

27.3.7.2 Configuring the maximum speed of the movement

The maximum speed or output frequency of the movement is configured in order to protect the digital output, the actuator/drive being controlled and/or the mechanical system.

Name:
X3Cfo_Mov01SpeedLimit
X3Cfo_Mov02SpeedLimit

These registers are used to configure the maximum speed / output frequency permitted in the system. It is important that the limit values for edge and pulse mode are different.

Edge mode

Data type	Value	Information
UDINT	10 to 400,000	Speed [increments per second]

Pulse mode

Data type	Value	Information
UDINT	5 to 200,000	Speed [increments per second]

27.3.7.3 Activates the movement

When a movement is active, the two channels are operated according to the preset values.

Name:
Mov01Enable
Mov02Enable

These registers are used to enable or disable the movement function.

Mov01Enable

Data type	Value	Information
USINT	0	Movement 1 disabled
	2	Movement 1 enabled: The speed setpoint is evaluated

Mov02Enable

Data type	Value	Information
USINT	0	Movement 2 disabled
	4	Movement 2 enabled: The speed setpoint is evaluated

27.3.7.4 Speed and direction control of the movement

The following parameters are important for speed and direction control of the movement:

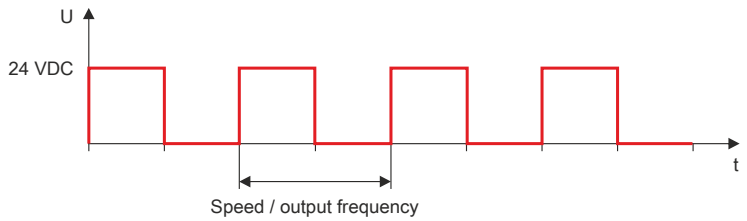
Characteristic value	Description
Speed control	The joint axes receive this speed setpoint from the standard application. 0 to ±32767 correspond to 0 to ±100% of the configured maximum speed
Direction control	The direction of movement is defined by the sign of the speed setpoint: 0 to +32767 correspond to 0 to the maximum speed in the positive direction of movement 0 to -32767 correspond to 0 to the maximum speed in the negative direction of movement
Resolution of the speed setpoint	The resolution of the speed setpoint is: Maximum speed / 32767
Relationship: Speed / Frequency	The relationship between speed and output frequency is: (Speed setpoint / Maximum speed) * 32767 

Table 23: Parameters for speed and direction control of the movement

Name:
Mov01Speed
Mov02Speed

These registers are used to set the speed of the movement.

Data type	Value	Information
INT	0 to 32,767	Speed setpoint 0 to 100%: Movement output F = 0 to maximum speed
		Positive direction of movement: Movement output D = 0
	0 to -32,767	Speed setpoint 0 to 100%: Movement output F = 0 to maximum speed
		Negative direction of movement: Movement output D = 1

27.3.7.5 Position feedback for movement

The position feedback is represented by a fixed point value [16.16]:

- HighWord = whole number increments
- LowWord = positions after the decimal of the increments

Name:
Mov01Position
Mov02Position

These registers show the current position of the movement.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Position value in fixed point format [16.16]